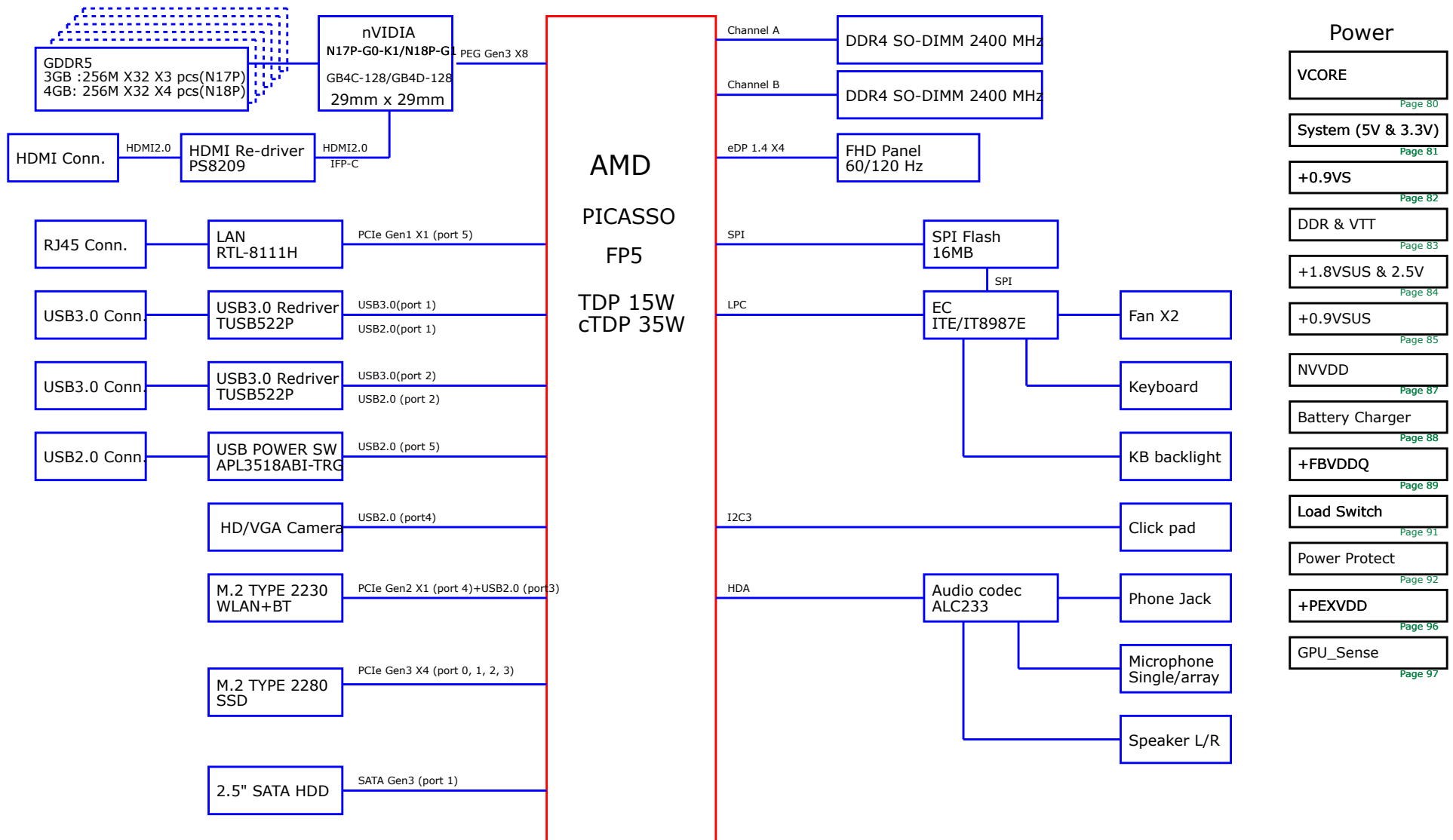
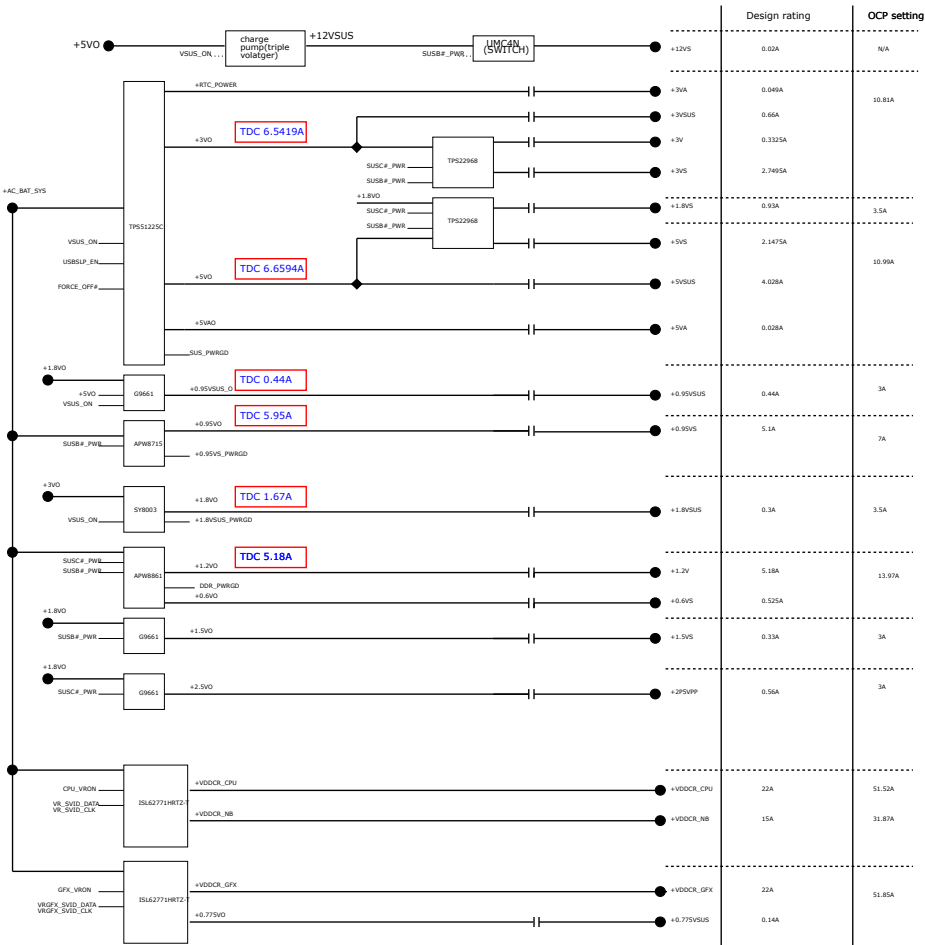
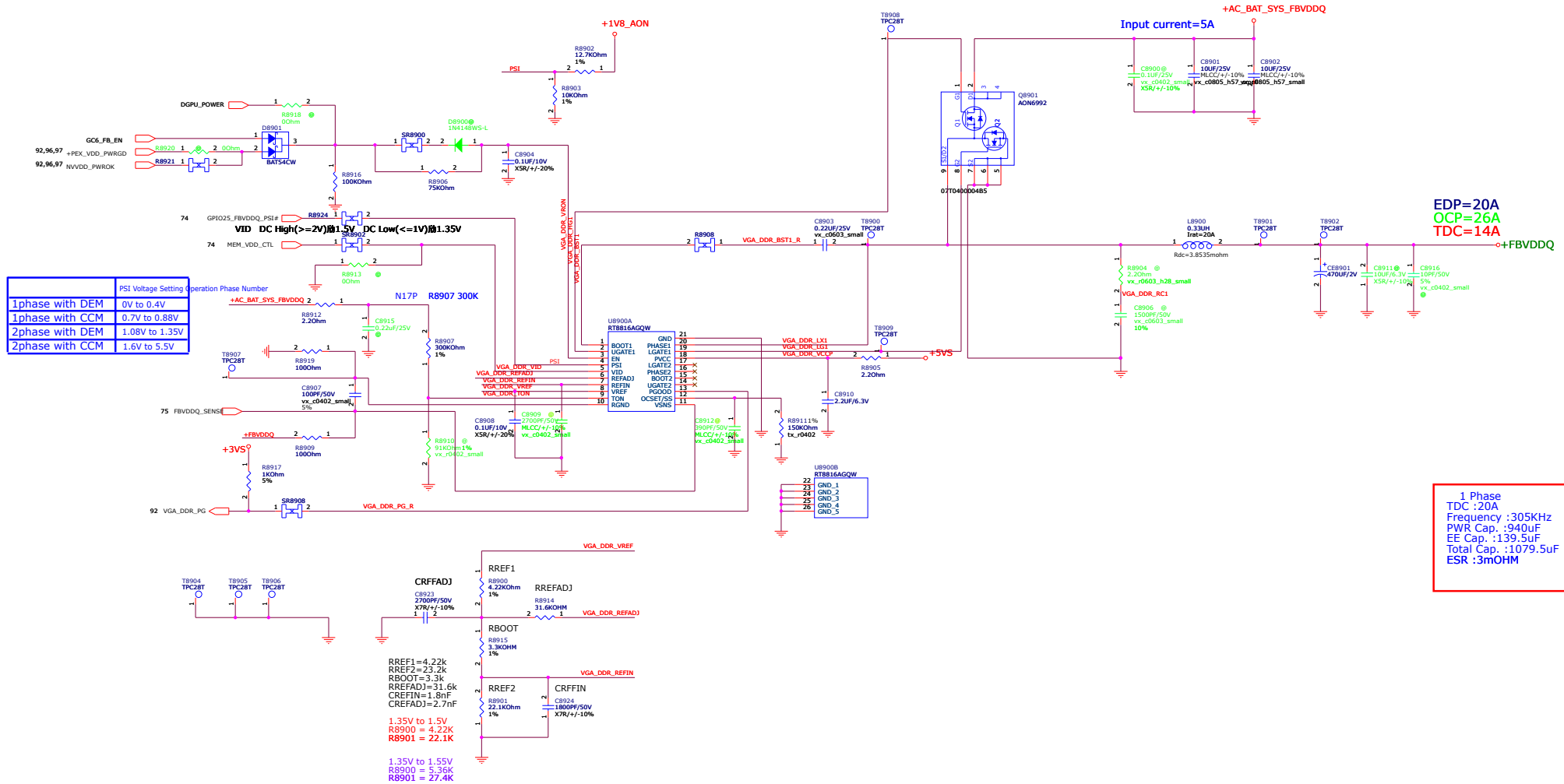


FX505DD/DT Block Diagram



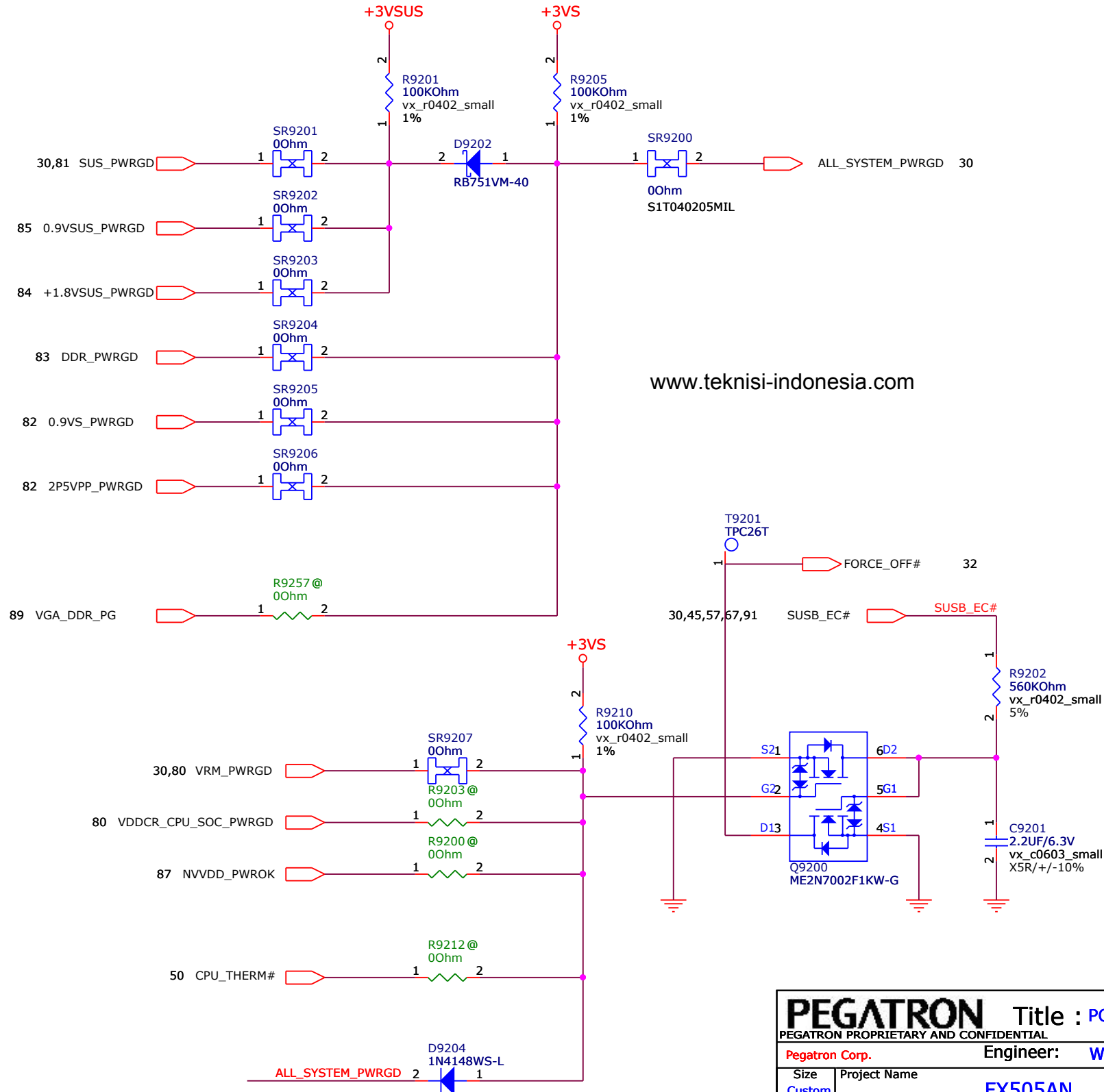


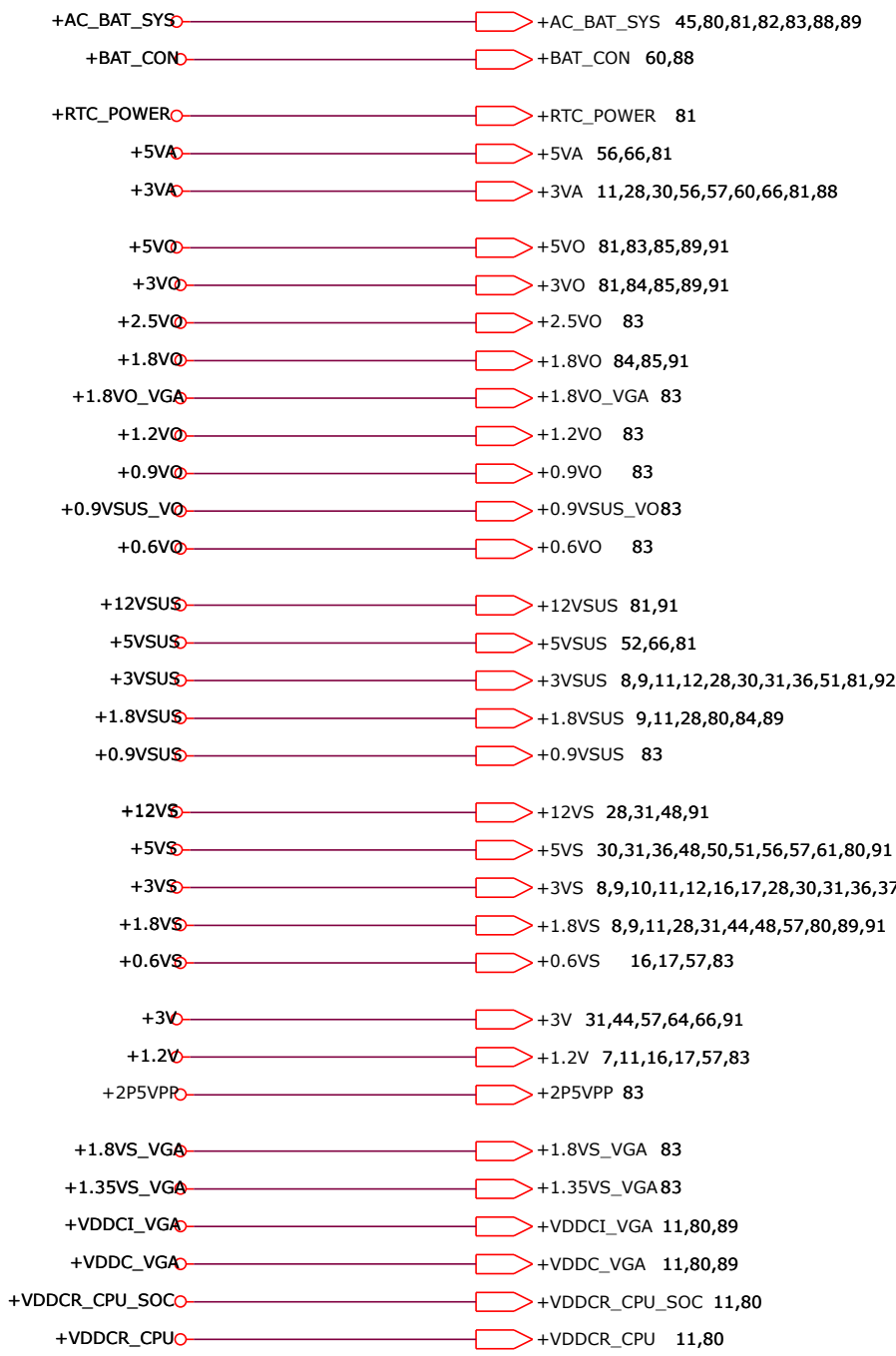
+FBVDDQ POWER SUPPLY



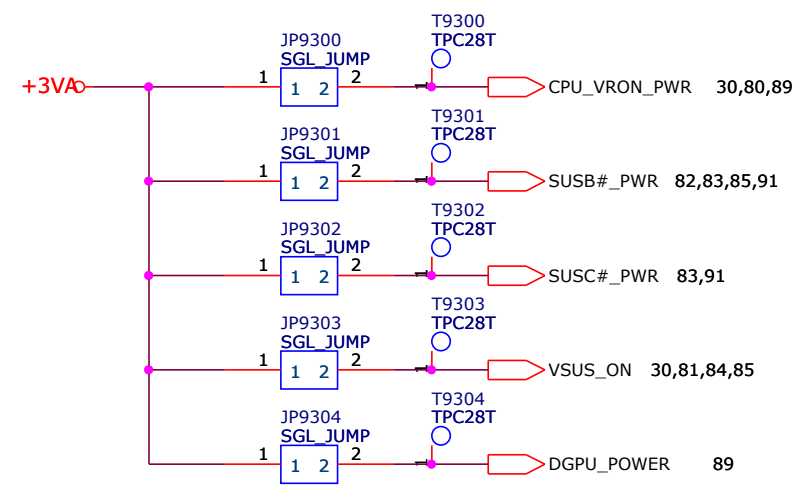
1 Phase
TDC :20A
Frequency :305KHz
PWR Cap. :940uF
EE Cap. :139.5uF
Total Cap. :1079.5uF
ESR :3mOHM

POWER GOOD DETECTOR

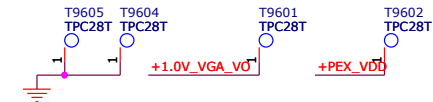
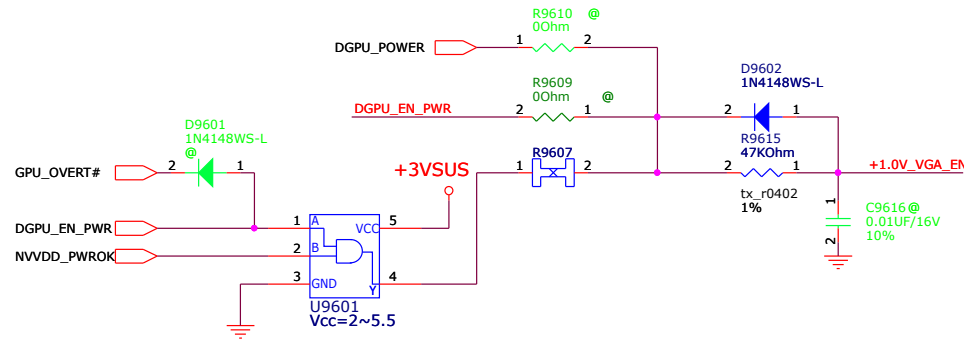
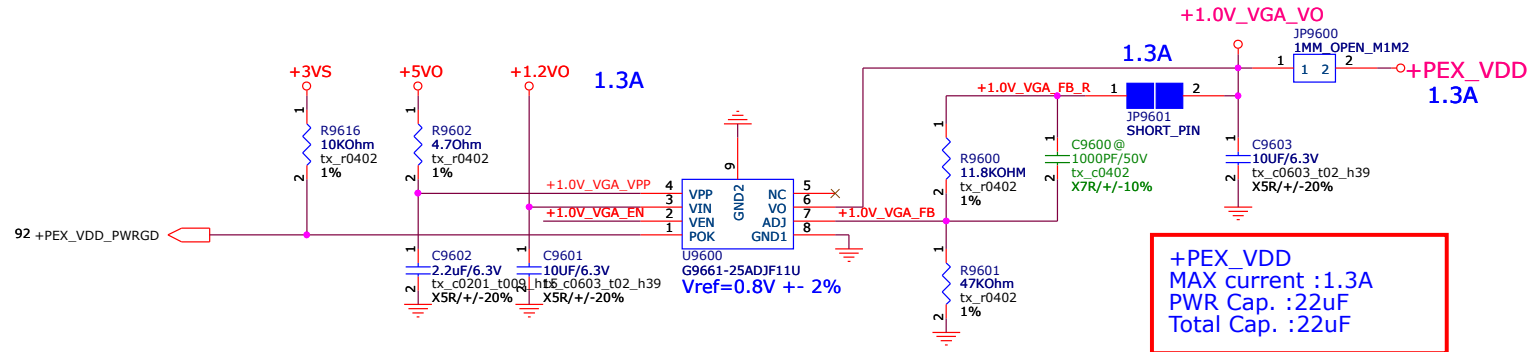


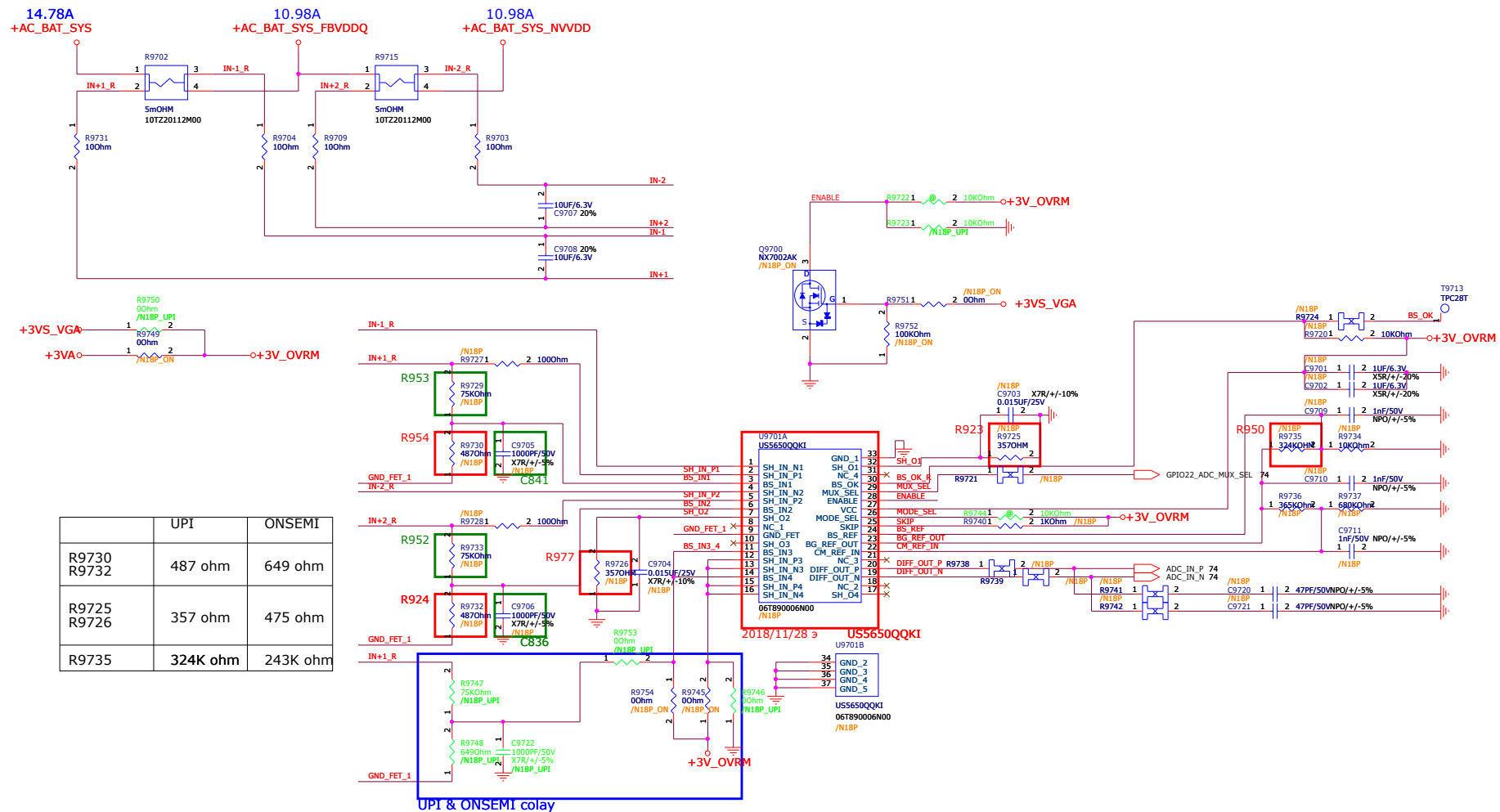


FOR POWER TEST



+PEX_VDD POWER SUPPLY





	UPI	ONSEMI
R9730 R9732	487 ohm	649 ohm
R9725 R9726	357 ohm	475 ohm
R9735	324K ohm	243K ohm

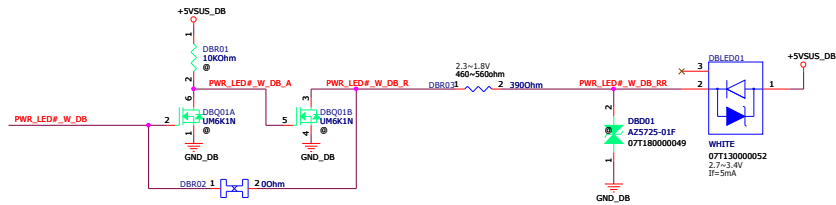
Table 12. Power Monitoring with OnSemi OVR-M

	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	649 Ω	475 Ω	243 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

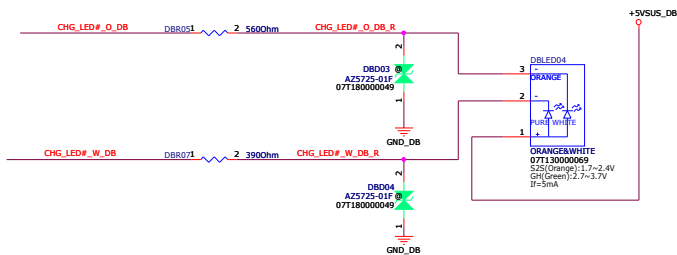
Table 13. Power Monitoring with uPI OVR-M

	Component Values				
GPU	R954, R924	R977, R923	R950	R953, R952	C841, C836
N18P-G0	487 Ω	357 Ω	324 kΩ	75 kΩ	1.0 nF
N18P-G0					
MAX-Q					

Power LED

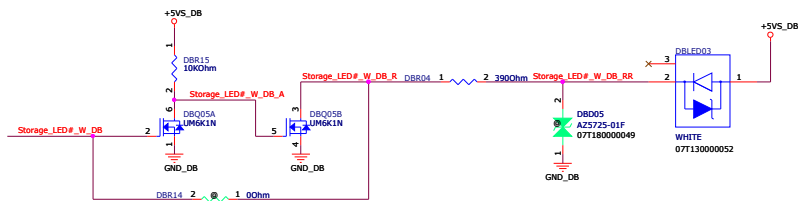


Charger LED(White/Orange)

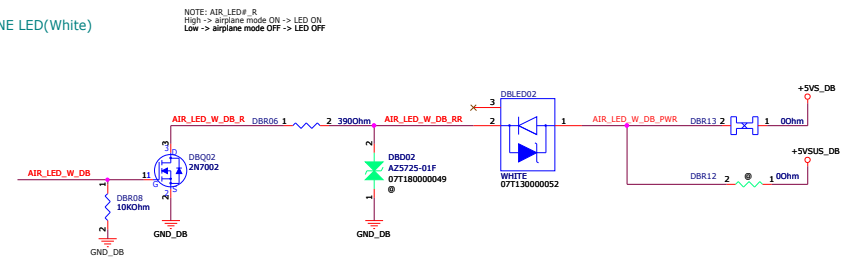


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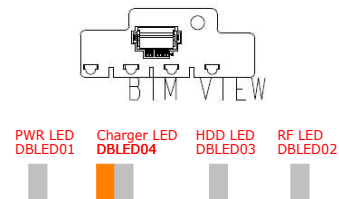
HDD LED



AIR PLANE LED(White)



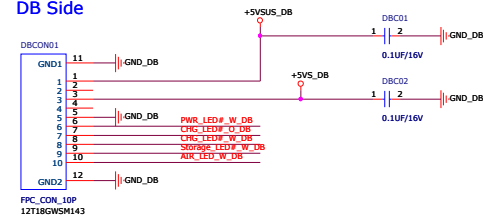
PCB/ID LOCATION



Tooling Hole



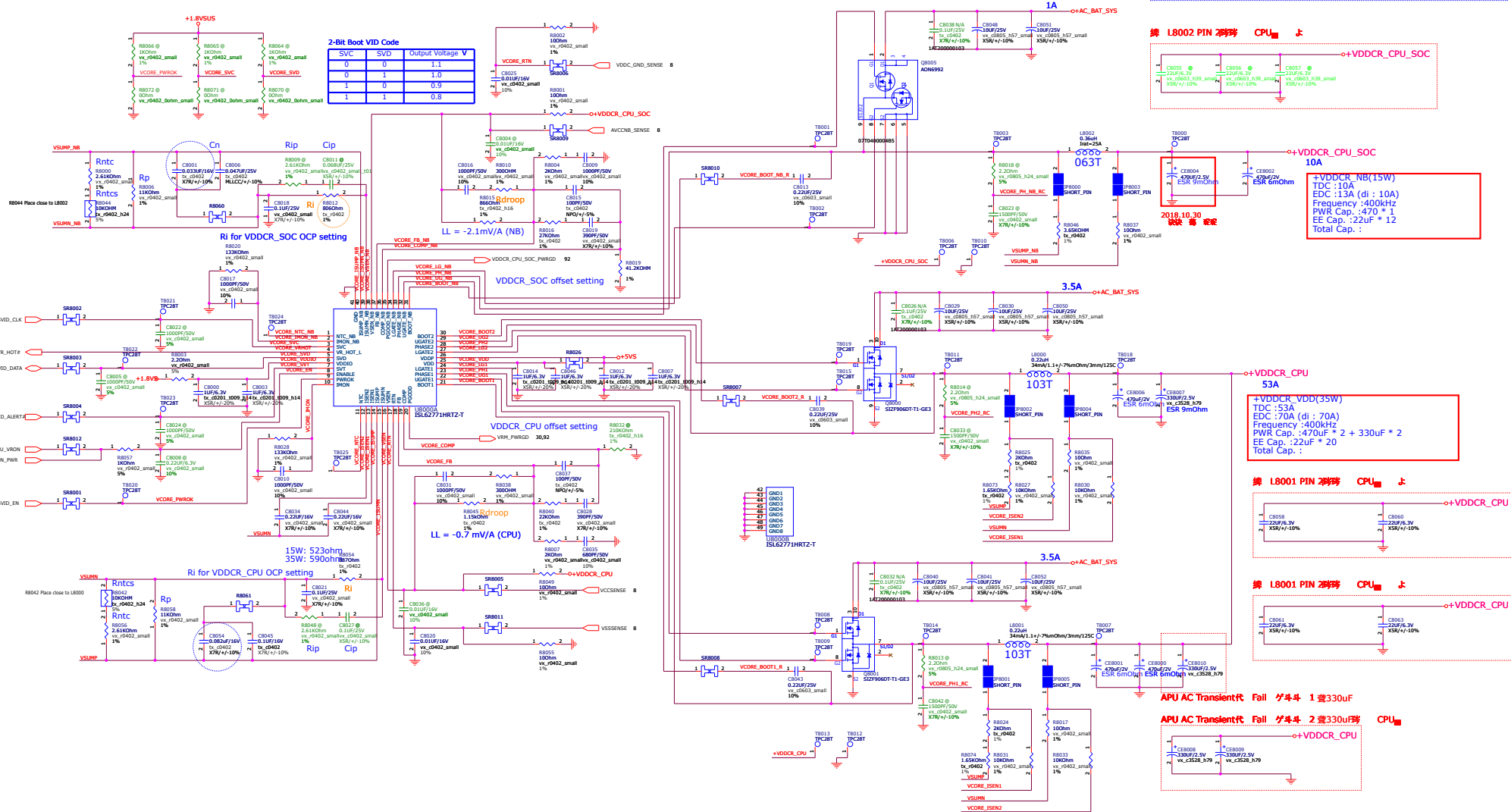
DB Side

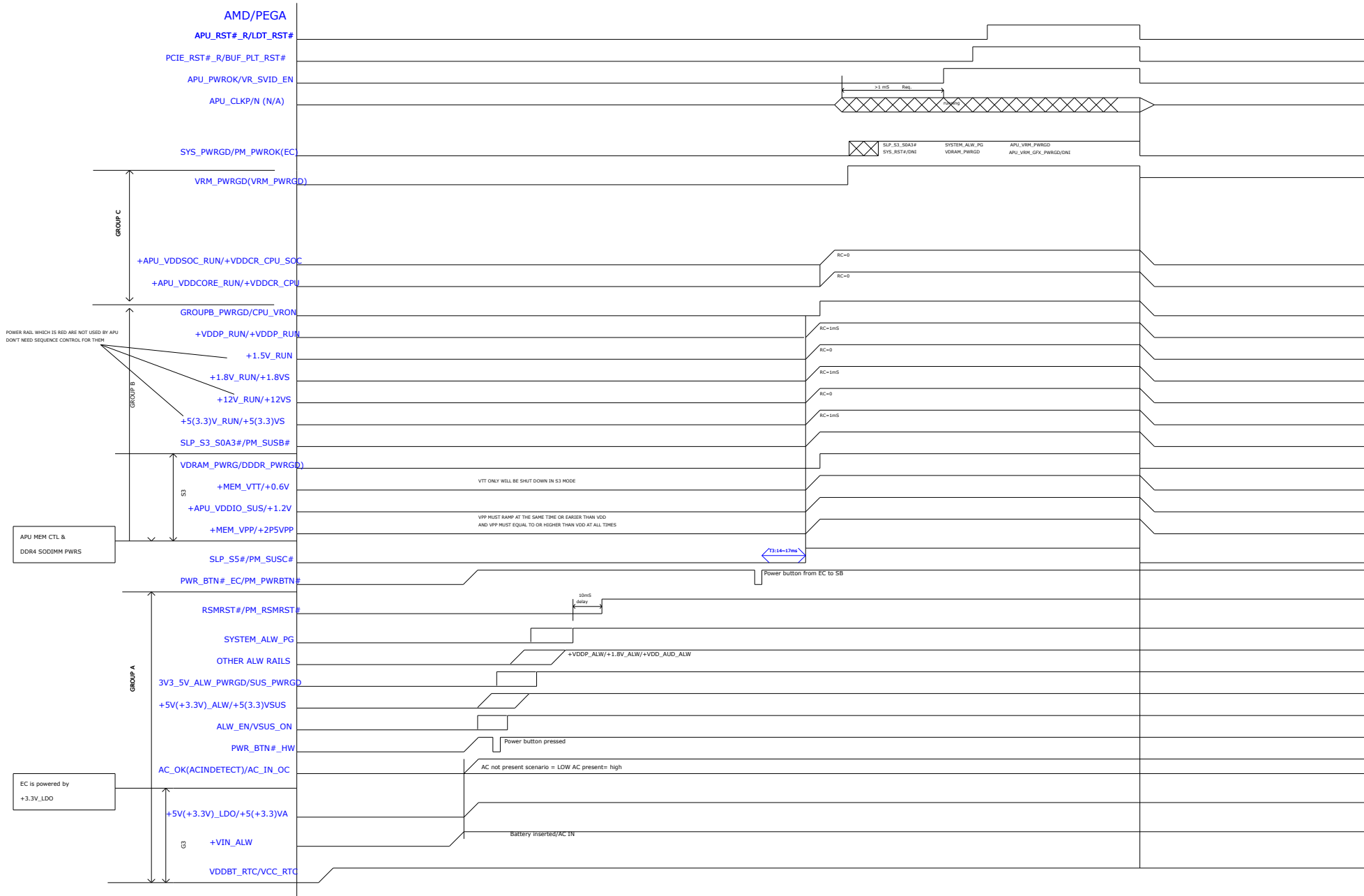


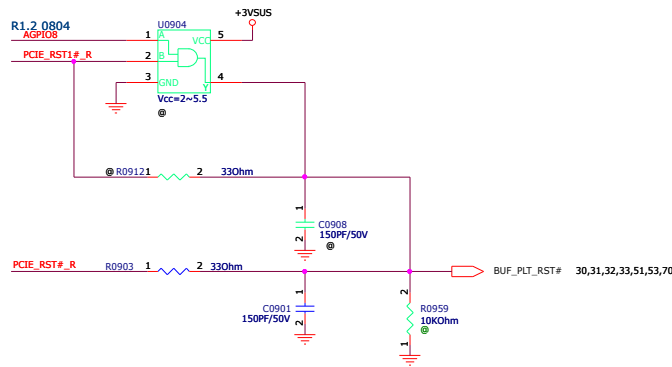
+5VSUS 11,31,56,81
+5VS 36,48,50,51,56,57,80,87,89,91



35W VCORE POWER SUPPLY

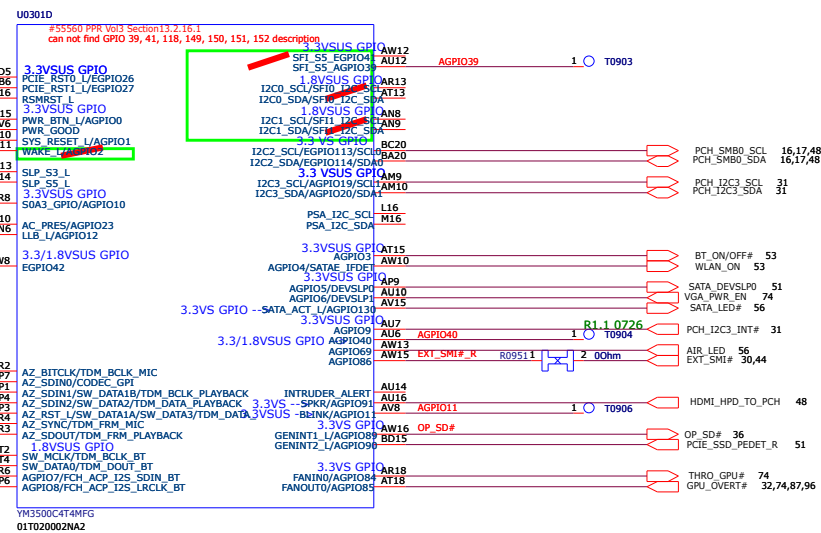
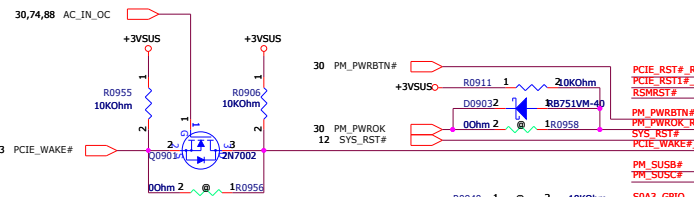
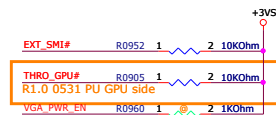
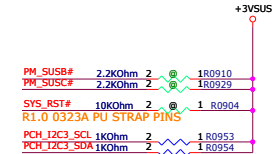




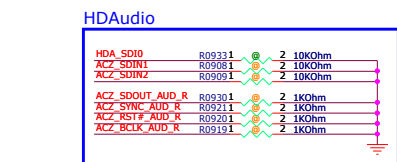


+1.8VSUS 8,11,12,24,28,36,57,80,91
 +3VS 8,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96
 +3VSUS 11,12,23,24,30,31,33,36,42,51,53,74,81,88,92,96

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SATA SSD1



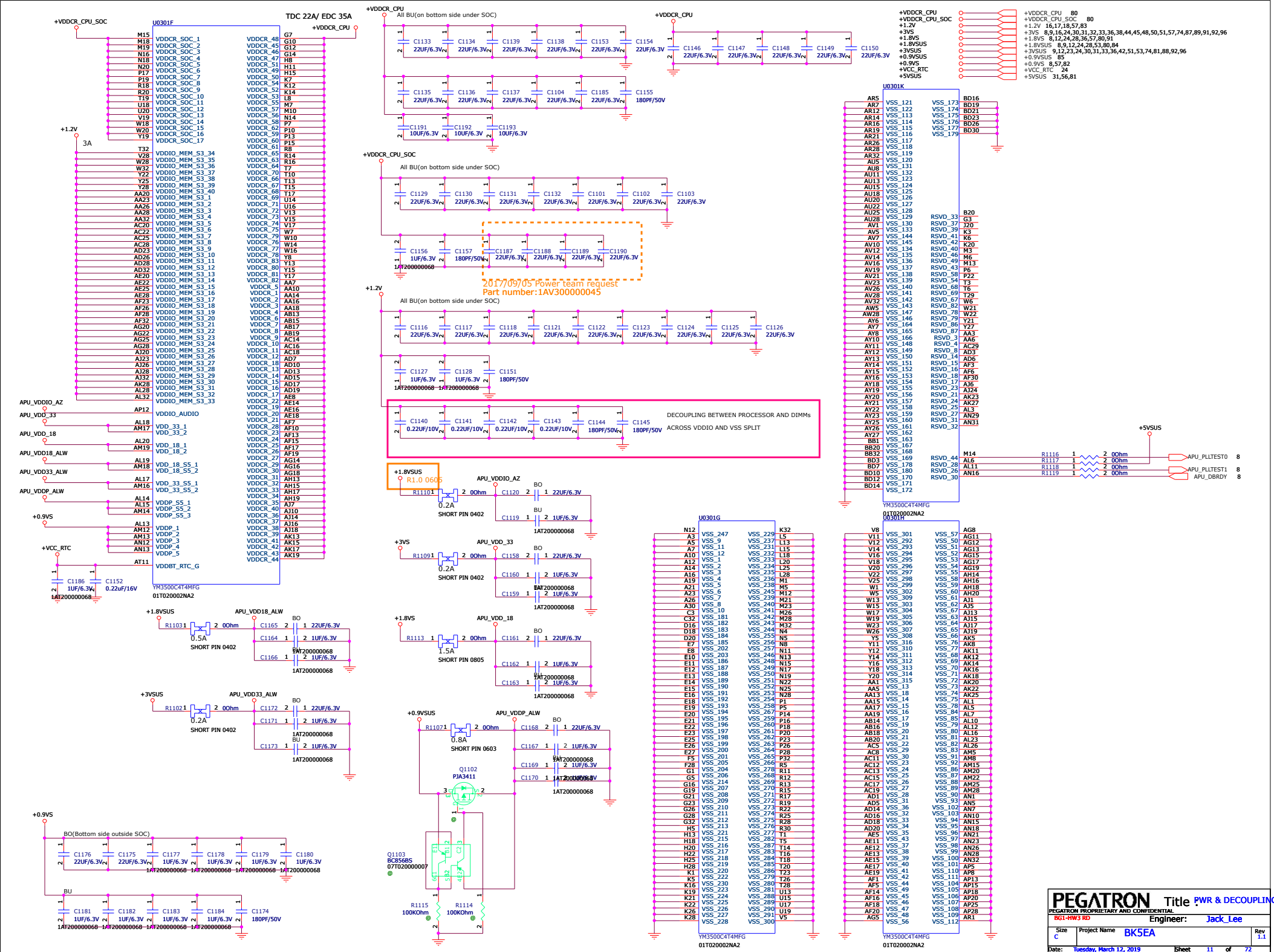
<Variant Name>

PEGATRON Title: EVENT_GPIO_SD_AZ
 PEGATRON PROPRIETARY AND CONFIDENTIAL

BGI-HW3 RD Engineer: Jack Lee

Size C Project Name BK5EA Rev 1.1

Date: Tuesday, March 12, 2019 Sheet 9 of 72

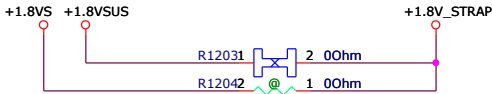


- +1.8VSUS

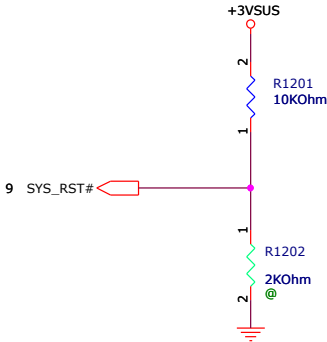
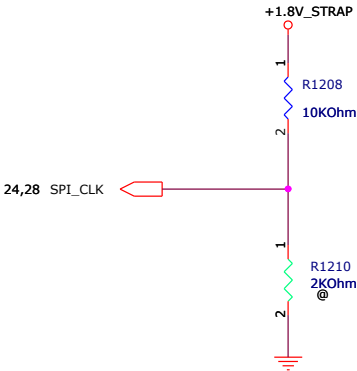
+1.8VSUS 8,9,11,24,28,53,80,84
- +1.8VS

+1.8VS 8,11,24,28,36,57,80,91
- +3VSUS

+3VSUS 9,11,23,24,30,31,33,36,42,51,53,74,81,88,92,96

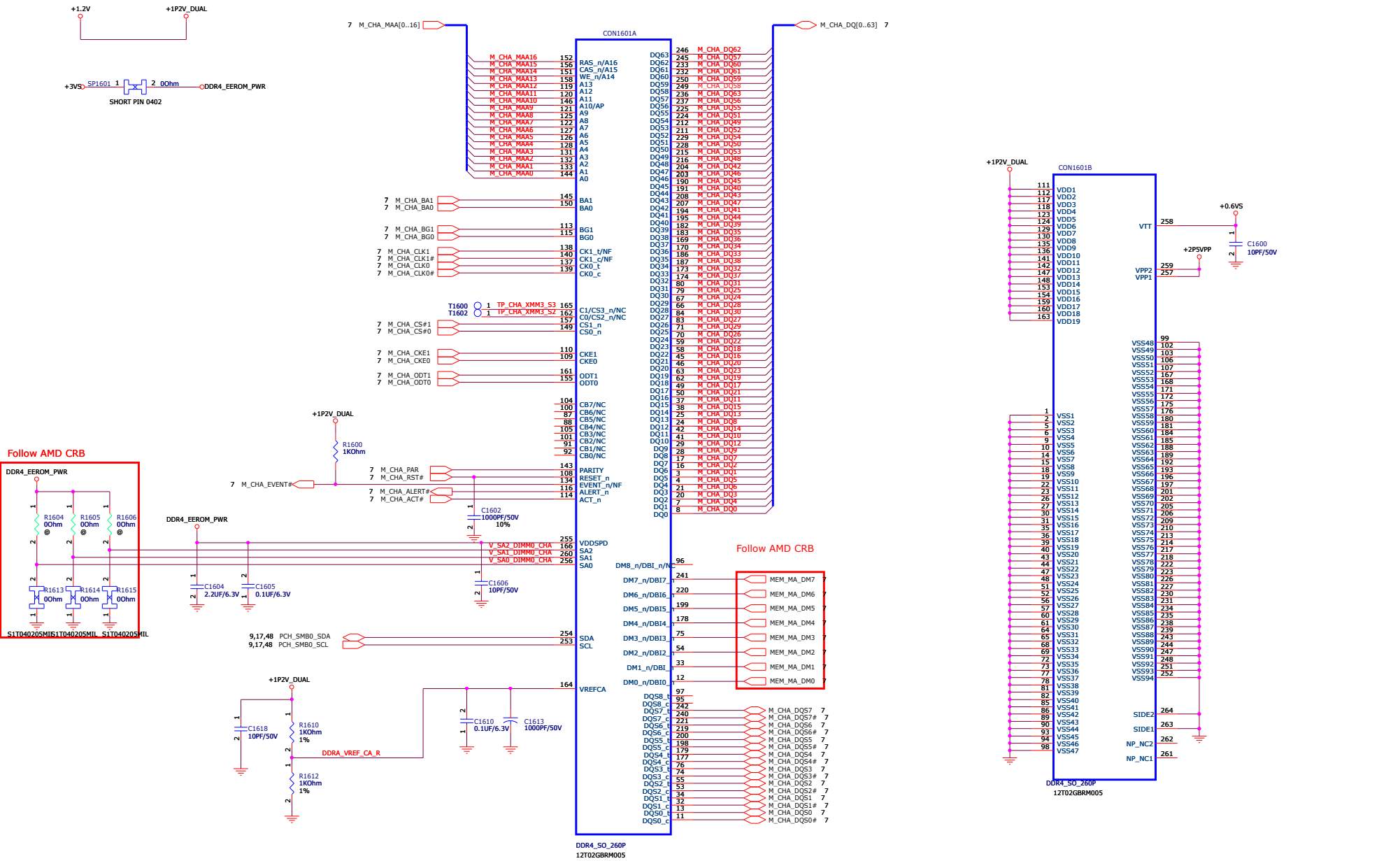


STRAP PINS

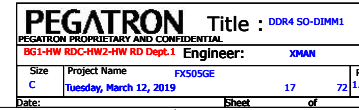


STRAP	FUNCTION	DEFINITION
SPI_CLK		1:USE 48MHZ CRYSTAL CLOCK AND GENERATE BOTH INTERNAL AND EXTERNAL CLOCKS(DEFAULT) 0:USE 100MHZ PCIE CLOCK AS REFERENCE CLOCK AND GENERATE INTERNAL CLOCKS ONLY
SYS_RST#		1:NORMAL RESET MODE(DEFAULT) 0:SHORT RESET MODE

DDR4 SO-DIMM 5.2H REV

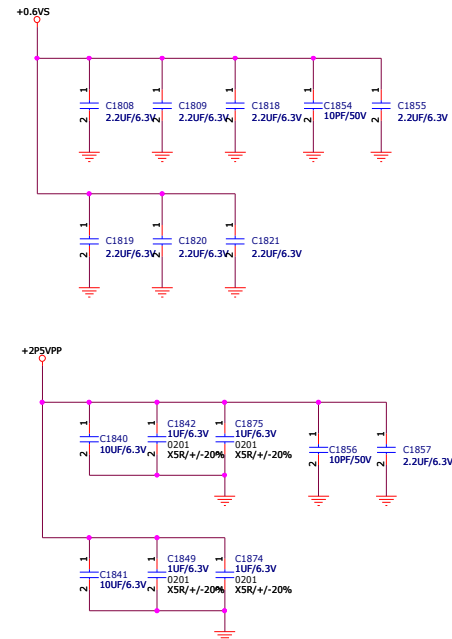
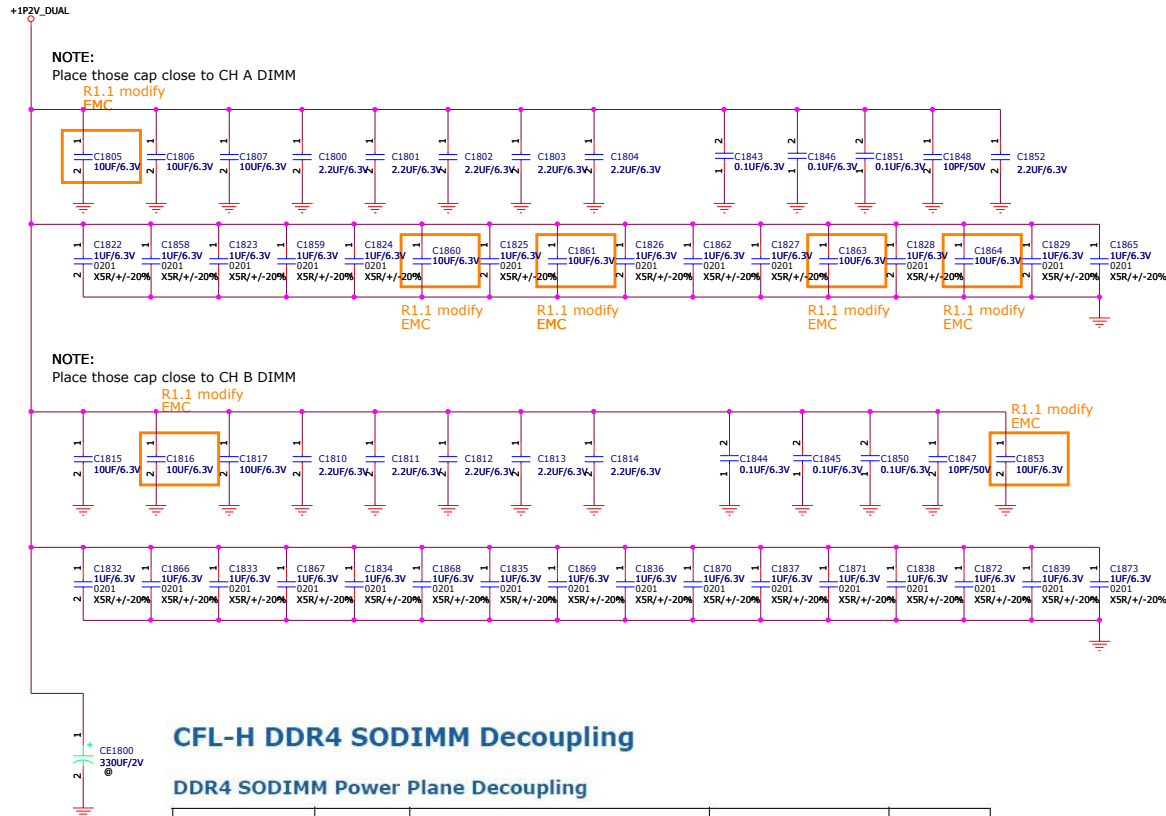


+1.2V	○					+1.2V	11,16,18,57,83
+1P2V_DUAL	○					+1P2V_DUAL	11,16,18,57,83
+0.6VS	○					+0.6VS	16,18,57,83
+2P5VPP	○					+2P5VPP	16,18,57,84
+3VS	○					+3VS	8,9,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96



+1.2V
 +1P2V_DUAL
 +0.6VS
 +2P5VPP
 +3VS

11,16,17,57,83
 11,16,17,57,83
 16,17,57,84
 16,17,57,84
 8,9,11,16,24,30,31,32,33,36,38,44,45,48,50,51,57,74,87,89,91,92,96

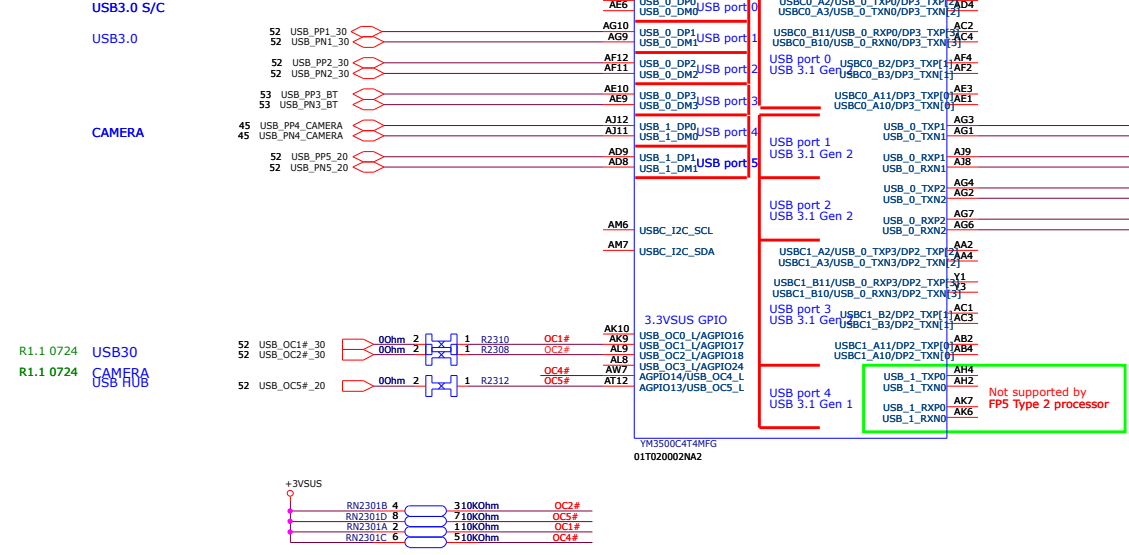
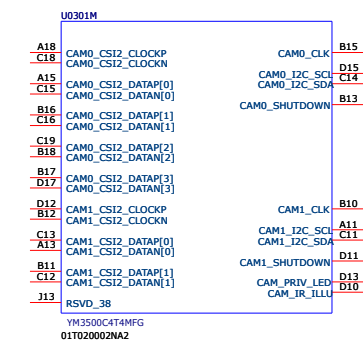
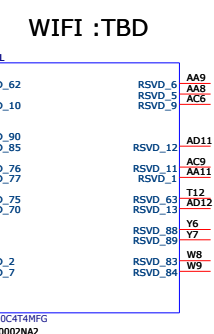
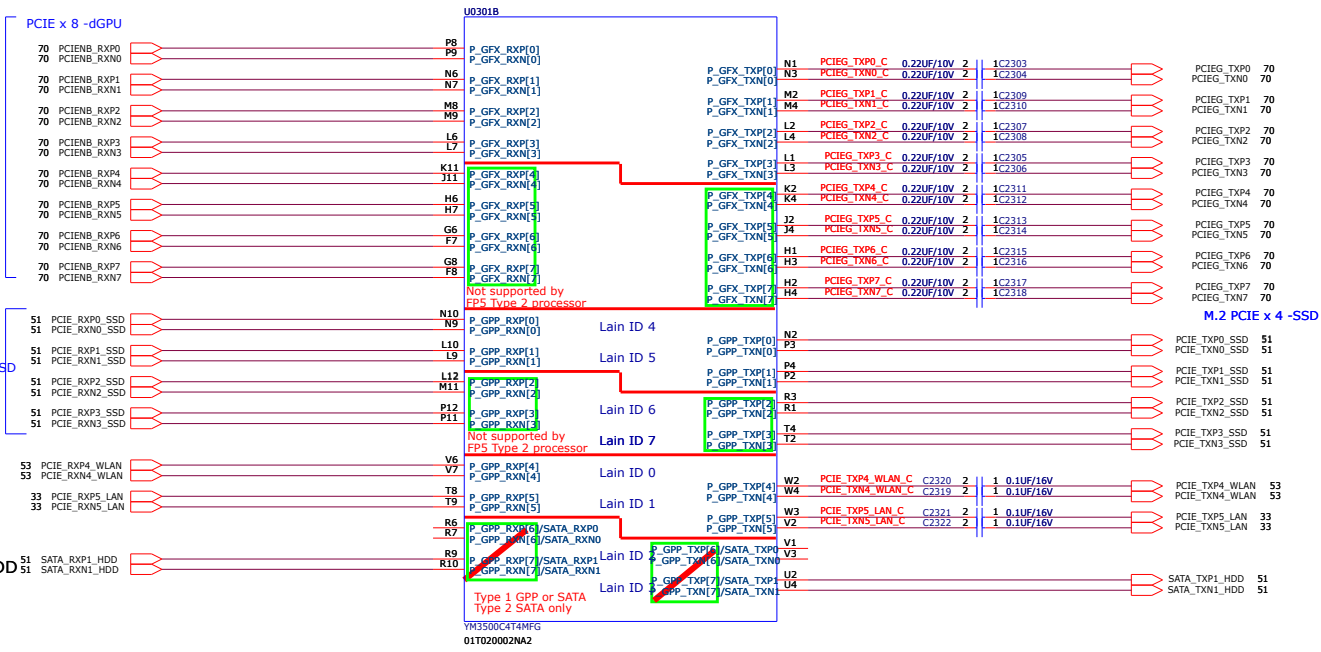


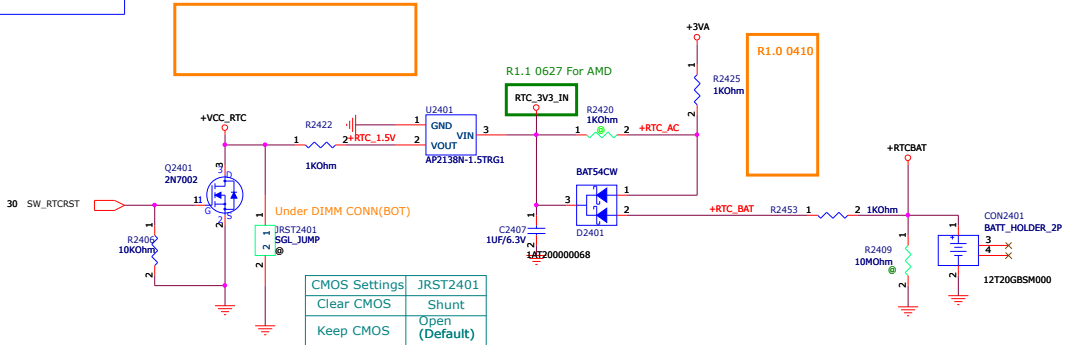
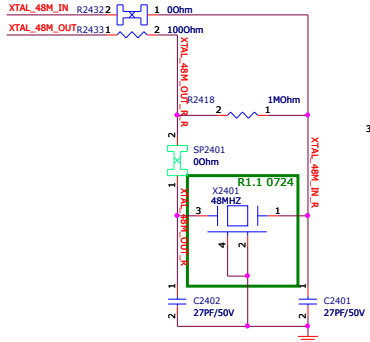
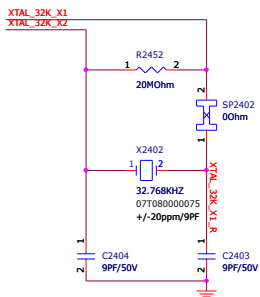
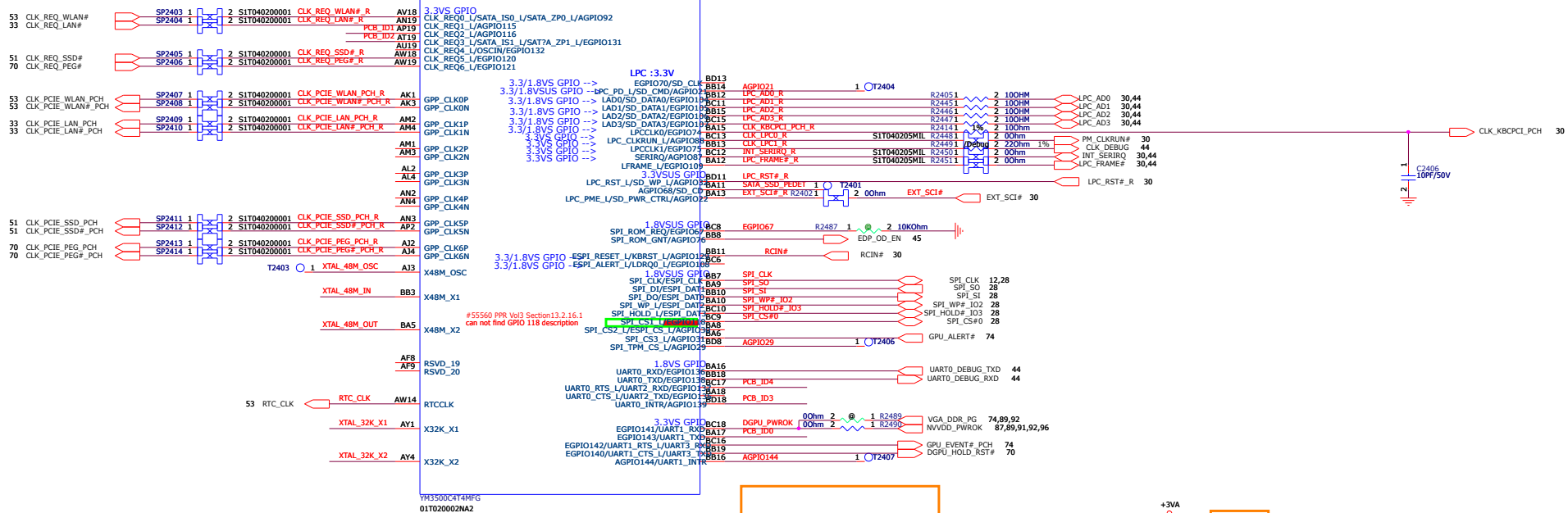
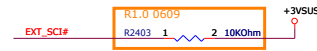
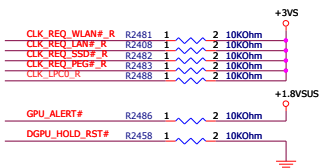
CFL-H DDR4 SODIMM Decoupling

DDR4 SODIMM Power Plane Decoupling

Memory Configuration	Power Domain	Decoupling Location	Qty x μ F (size)	Note
DDR4 2 Channels SODIMM 1DPC	VDDQ	4 near each side of the DIMM connector close to VDD pins	16x 10 μ F (0603)	
		4 near each side of the DIMM connector close to VDD pins	16x 1 μ F (0402)	
		1 placeholder	1x 330 μ F (7343)	
	VTT	Placed on VTT plane close to DIMM, 1 cap stuffed, 1 placeholder	2x 10 μ F (0603)	
		Placed on VTT plane close to DIMM	4x 1 μ F (0402)	
	VPP	DIMM Pin side, 1 per DIMM	2x 10 μ F (0603)	
		DIMM Pin side, 1 per DIMM	2x 1 μ F (0402)	
	VDDSPD	Place close to DIMM	2x 0.1 μ F (0402)	
		Place close to DIMM	2x 2.2 μ F (0402)	

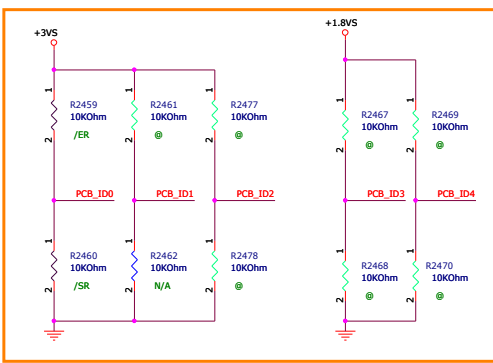
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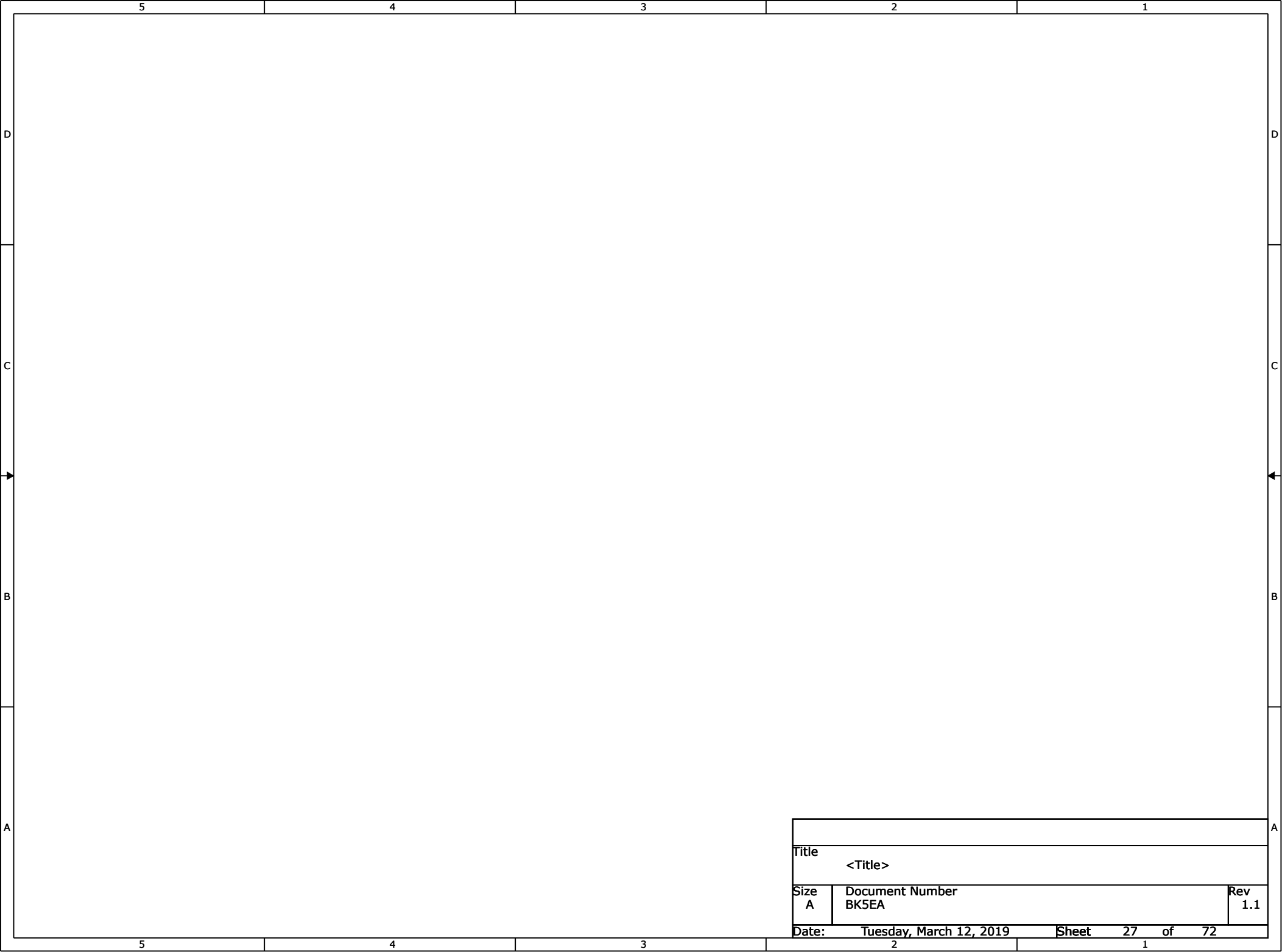


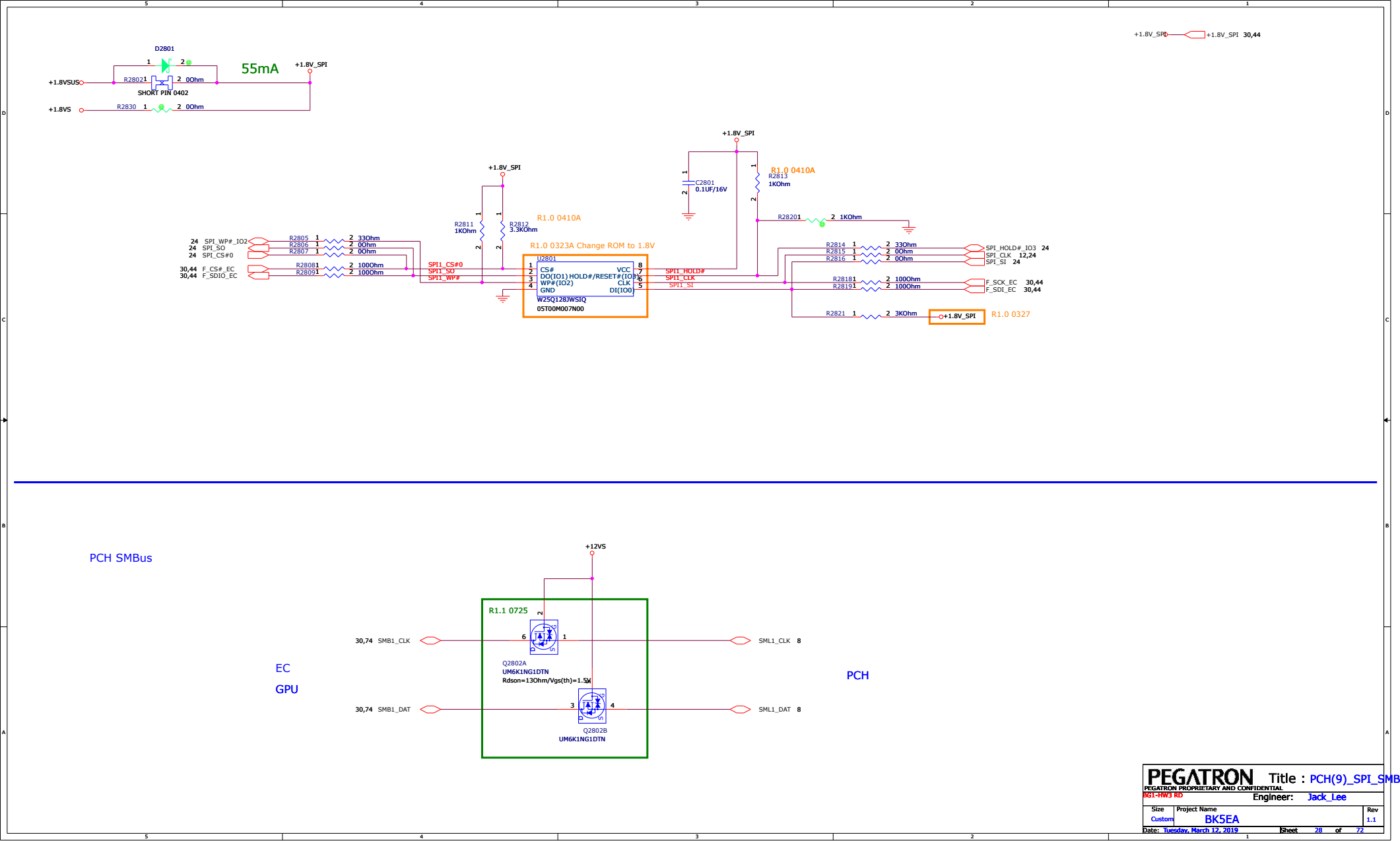


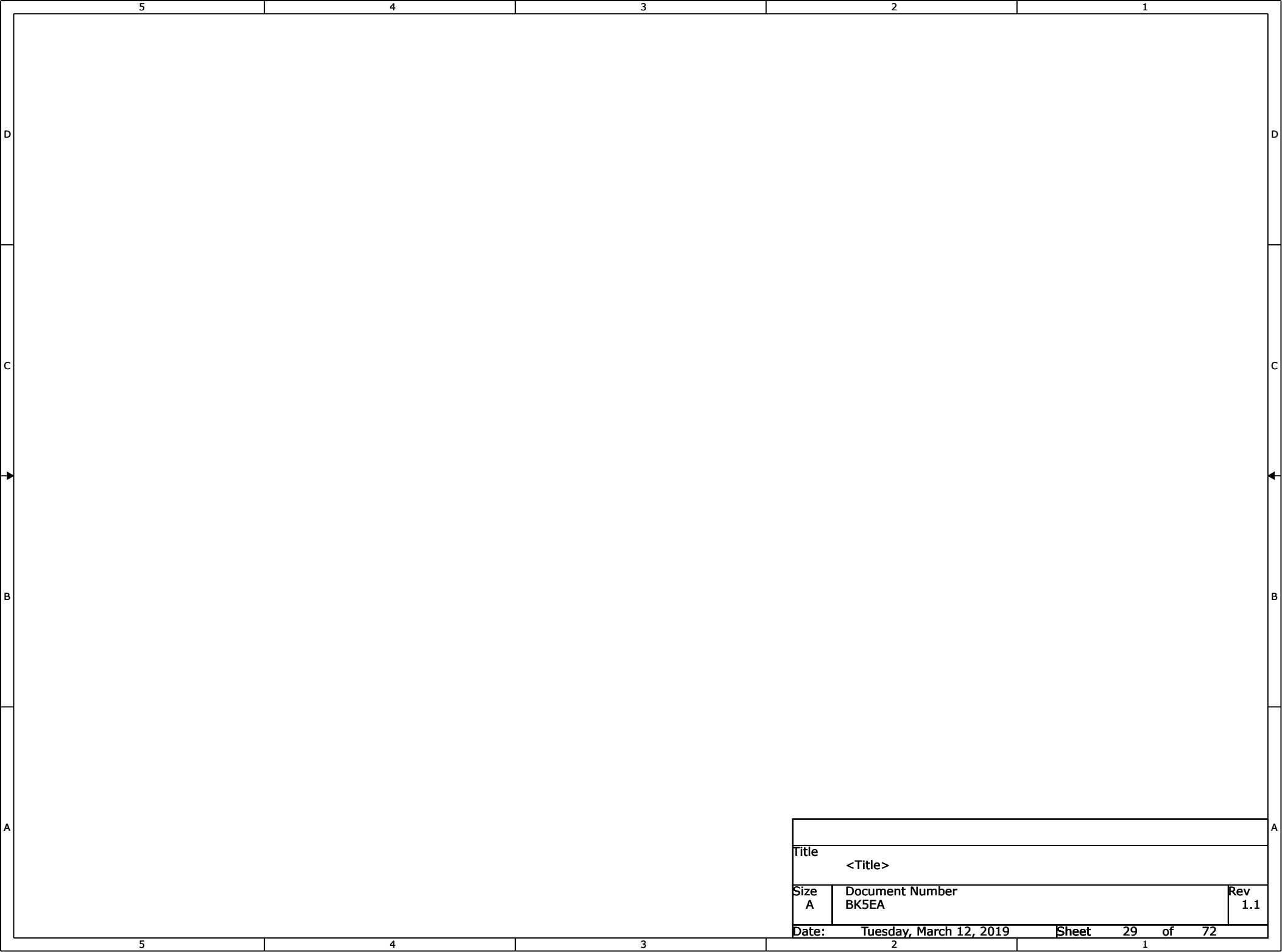
PCB ID	SR	ER
ID0	L	H
ID1	L	L

CMOS Settings	JRST2401
Clear CMOS	Shunt
Keep CMOS	Open (Default)

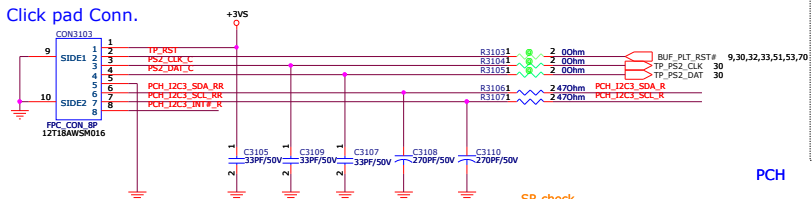




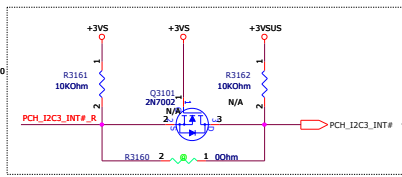




Click pad Conn.

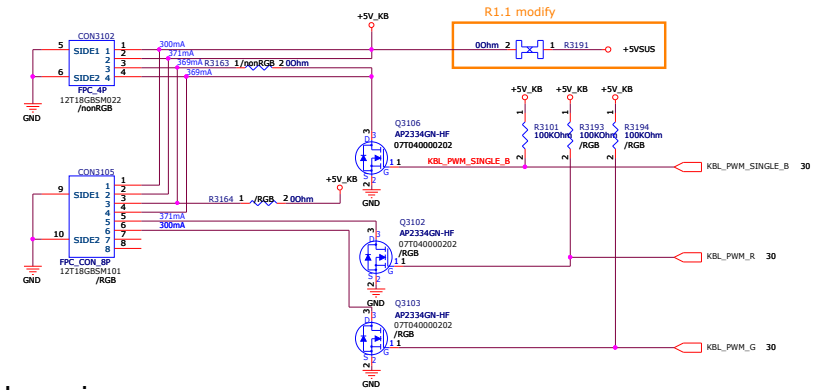


PCH



Click Pad

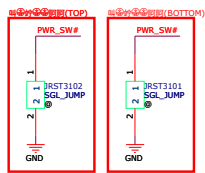
KB Backlight Conn.



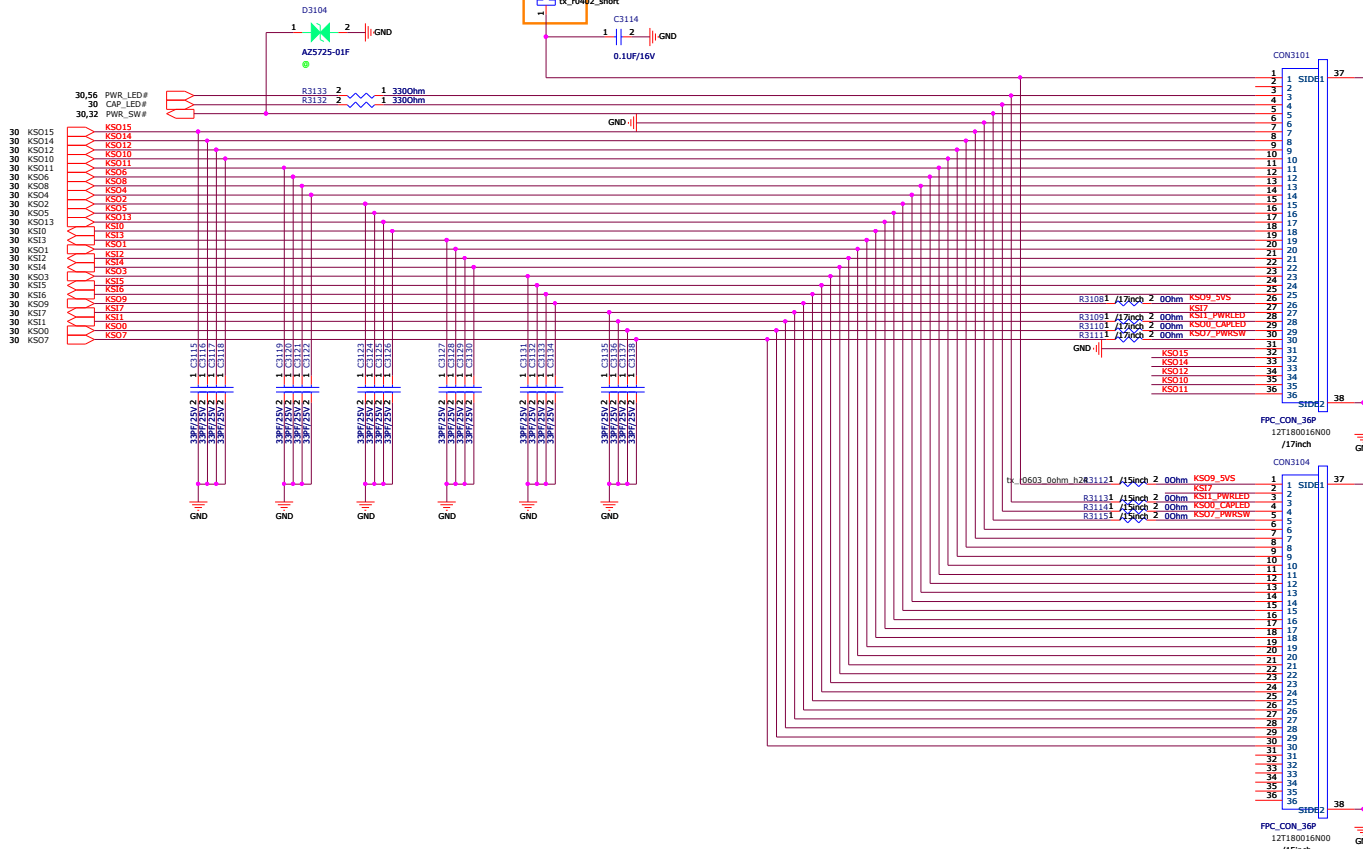
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Keyboard Conn.

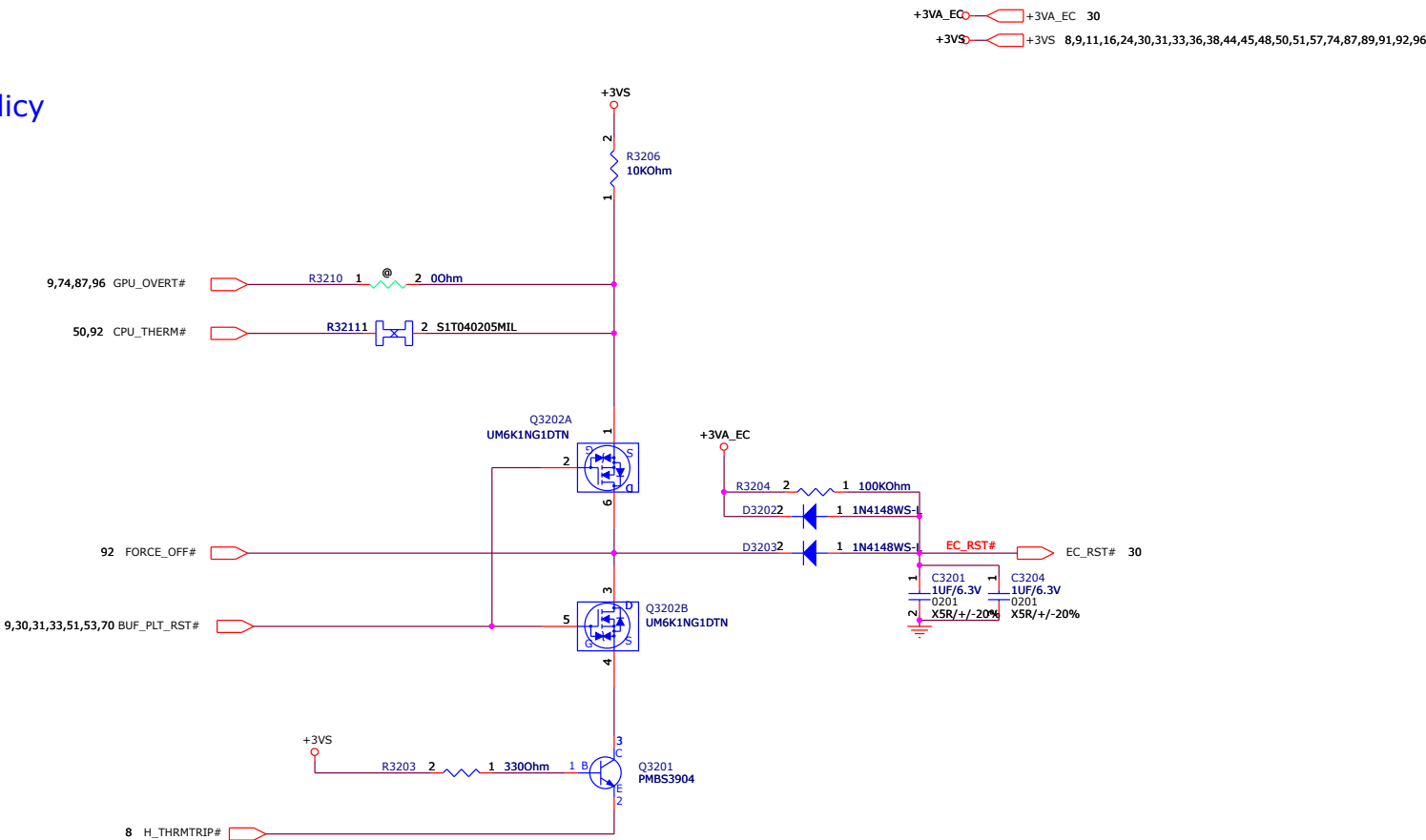
Power-on jumper



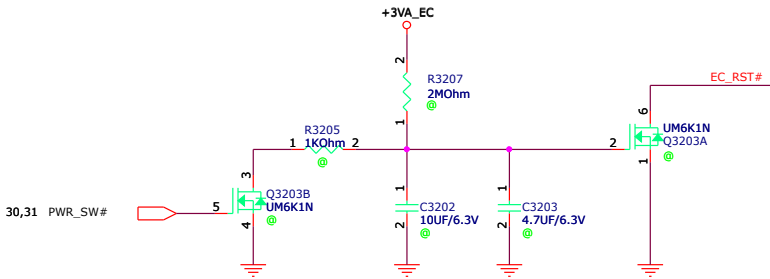
PIN 1	LED VCC
PIN 2	NC
PIN 3	Power LED
PIN 4	Capable LED
PIN 5	Power SW
PIN 6	Power GND
PIN 7	KS015
PIN 8	KS014
PIN 9	KS012
PIN 10	KS010
PIN 11	KS011
PIN 12	KS06
PIN 13	KS08
PIN 14	KS04
PIN 15	KS02
PIN 16	KS08
PIN 17	KS013
PIN 18	KS0
PIN 19	KS13
PIN 20	KS01
PIN 21	KS2
PIN 22	KS4
PIN 23	KS03
PIN 24	KS05
PIN 25	KS09
PIN 26	KS08
PIN 27	KS07
PIN 28	KS11
PIN 29	KS00
PIN 30	KS07
PIN 31	NC
PIN 32	NC
PIN 33	NC
PIN 34	NC
PIN 35	NC
PIN 36	NC



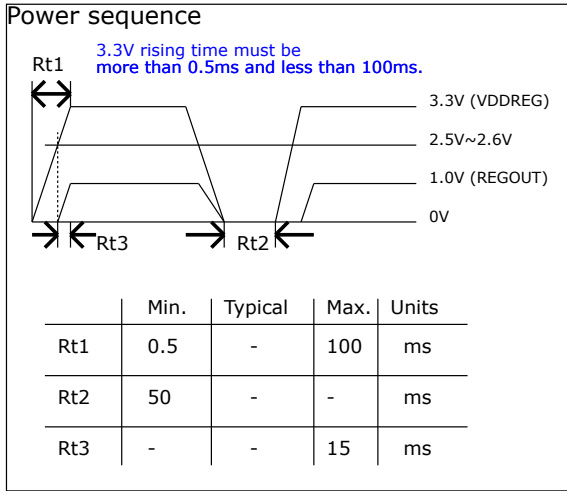
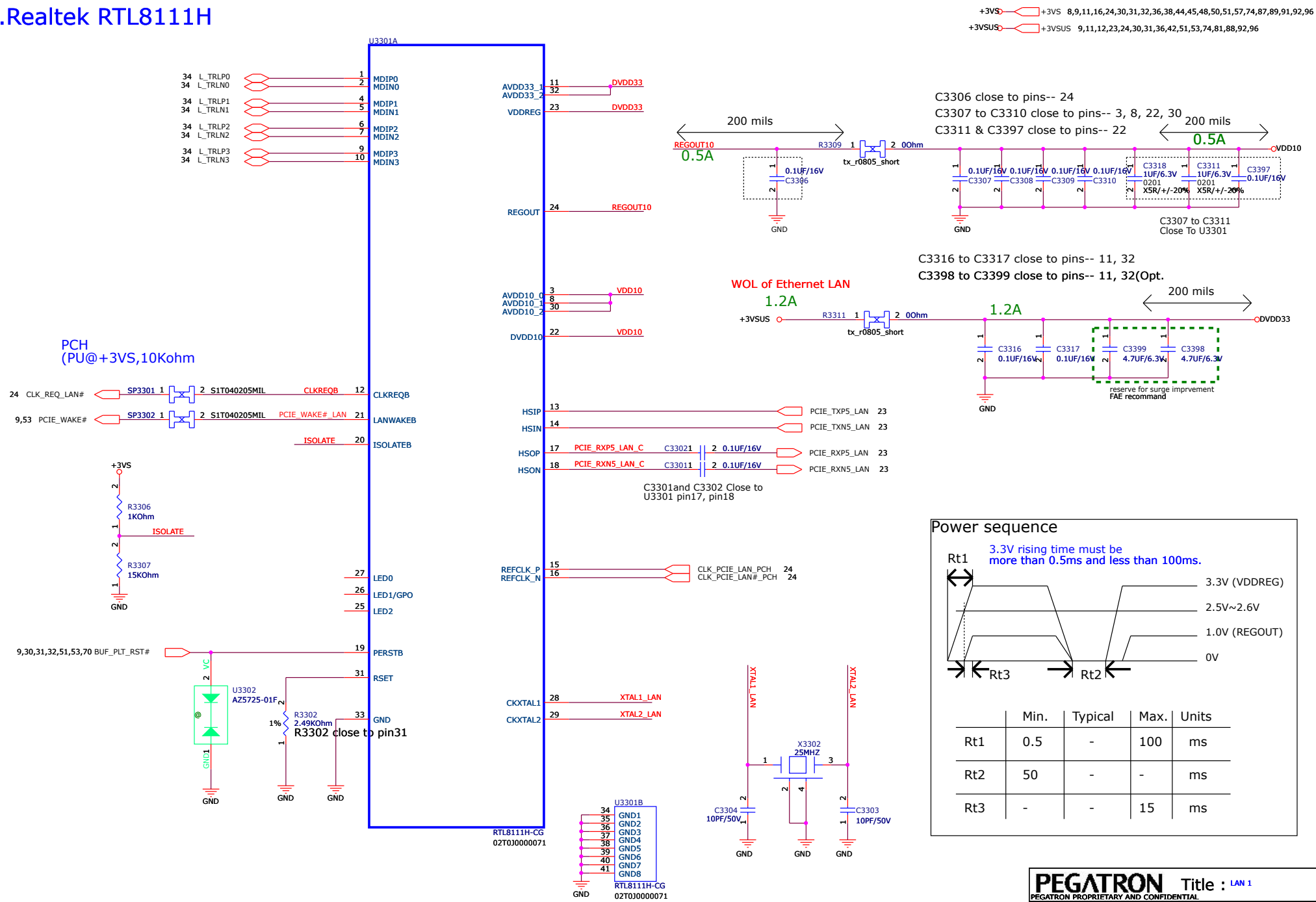
Thermal Policy



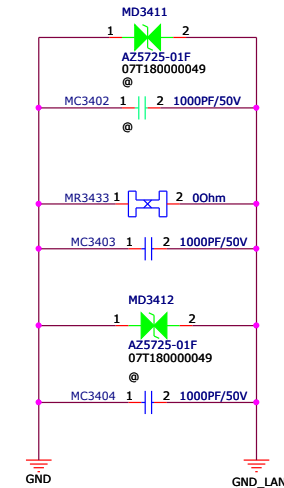
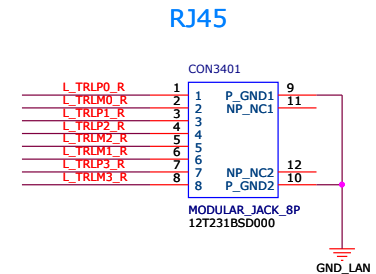
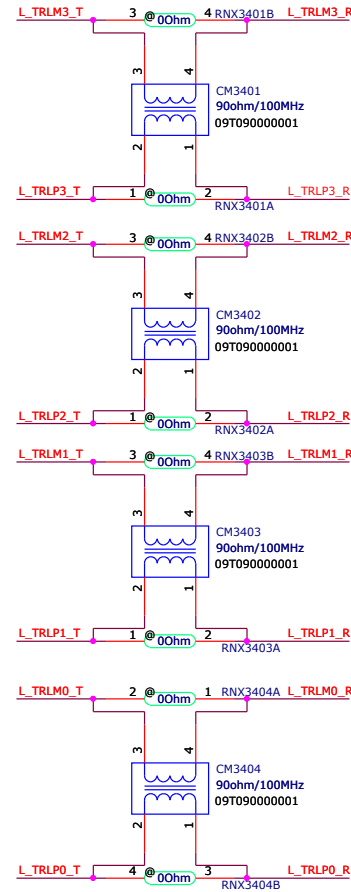
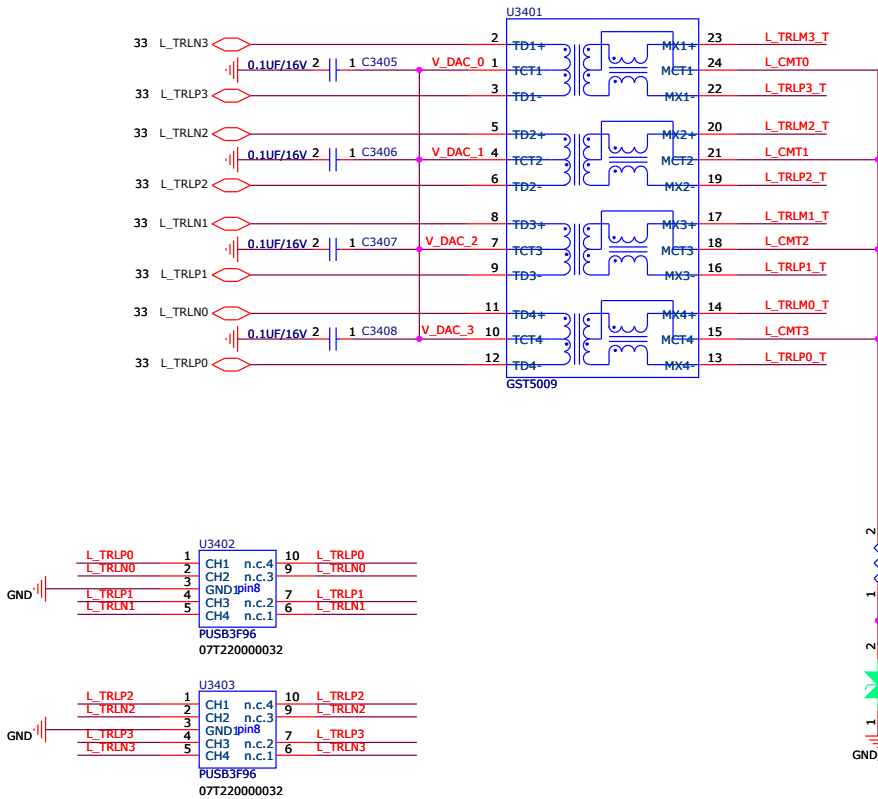
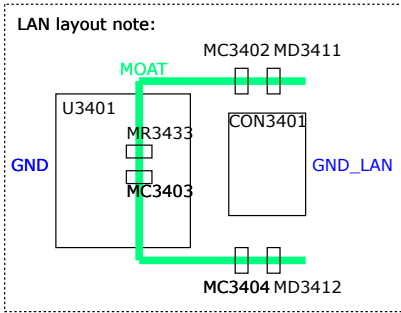
EC reset



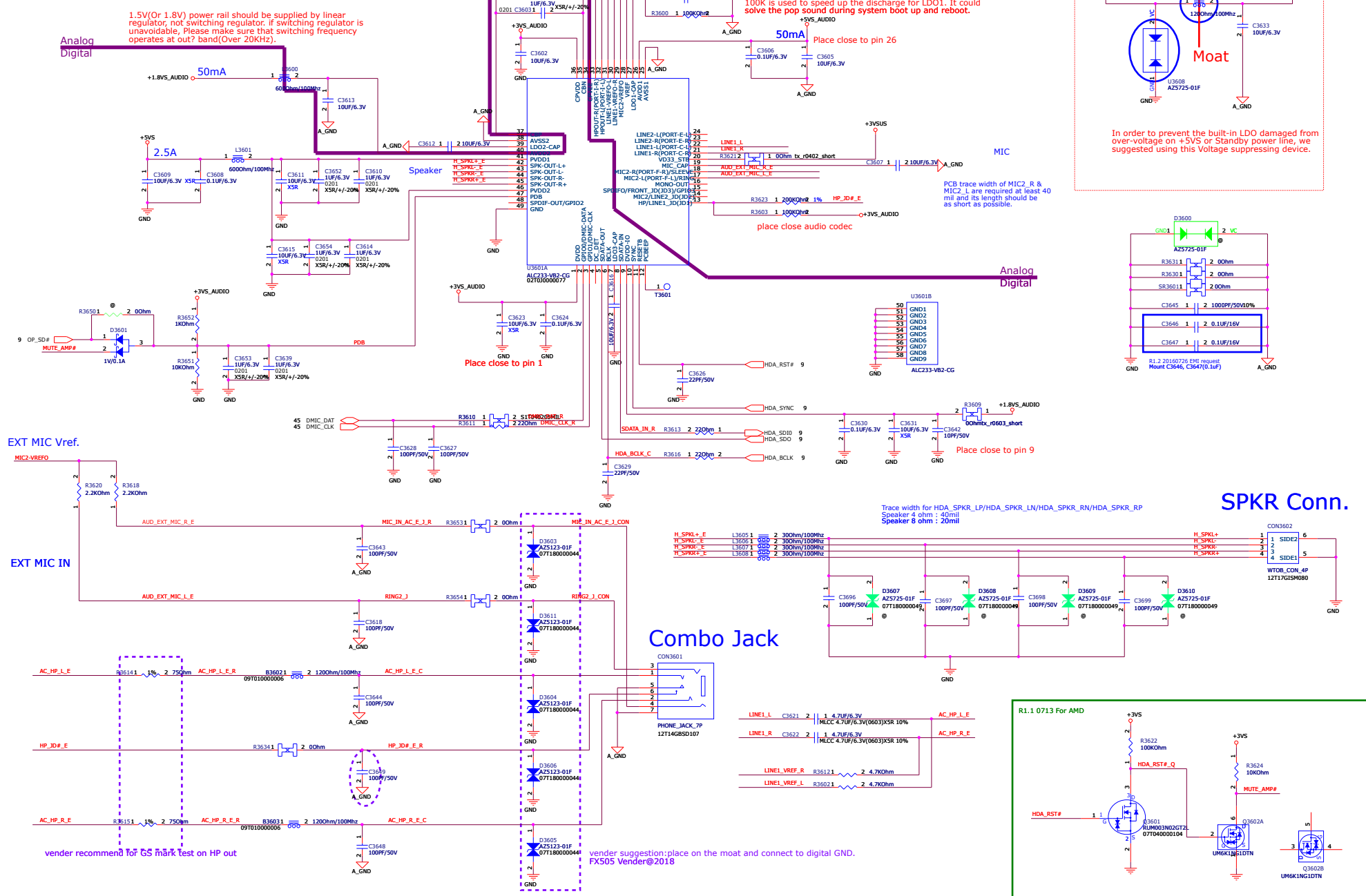
33.Realtek RTL8111H



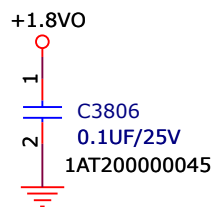
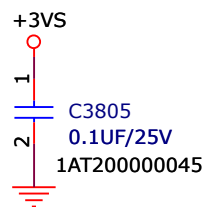
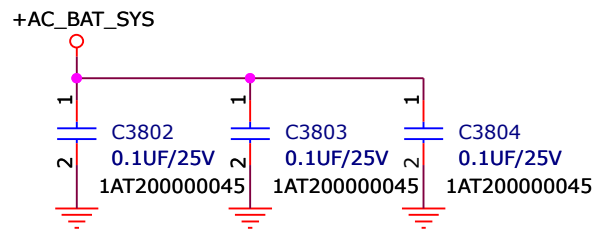
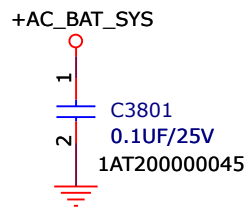
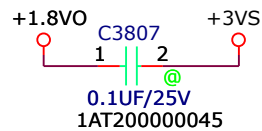
34. Transformer/RJ45



ALC233-VB2-CG CODEC

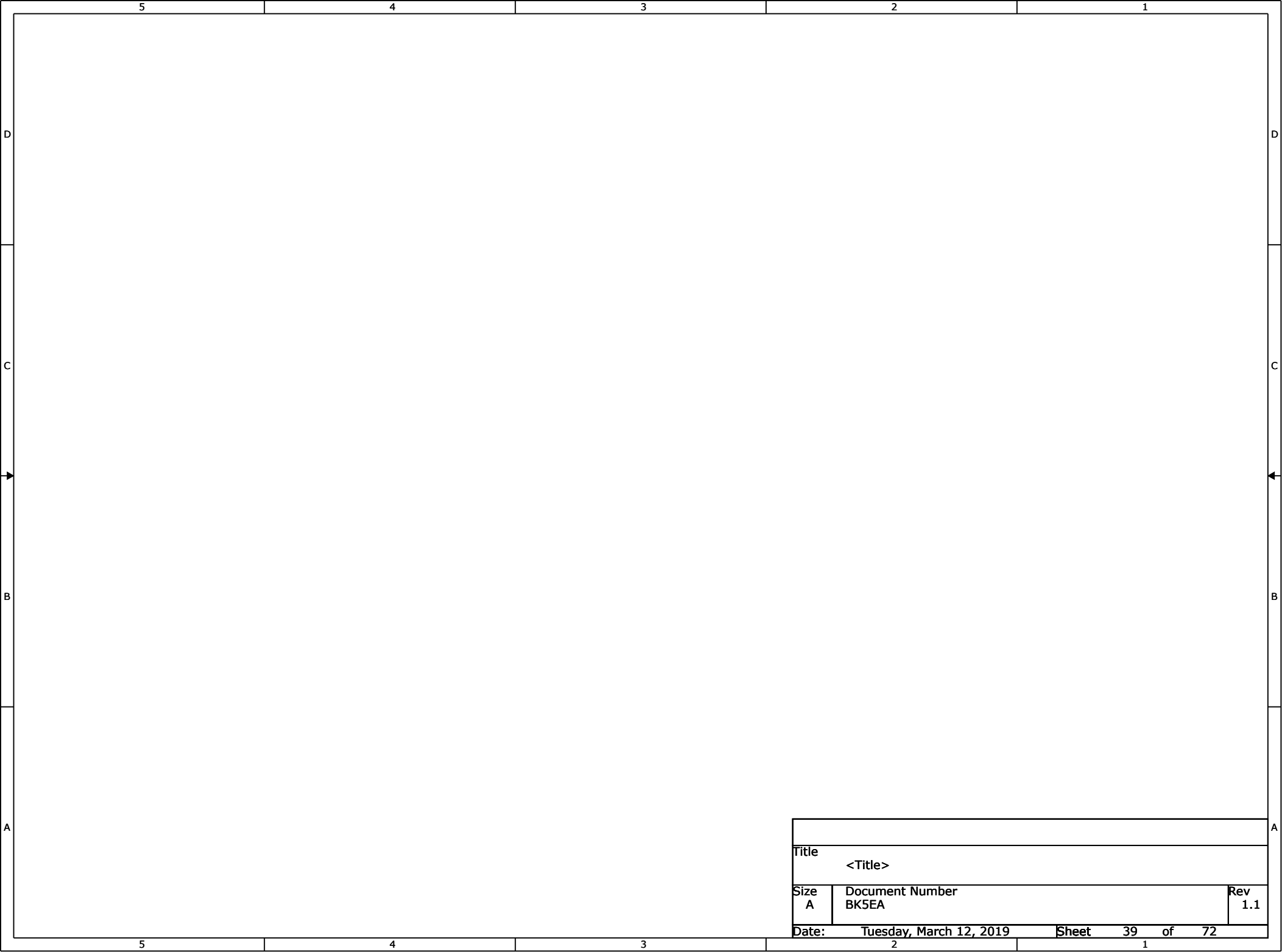


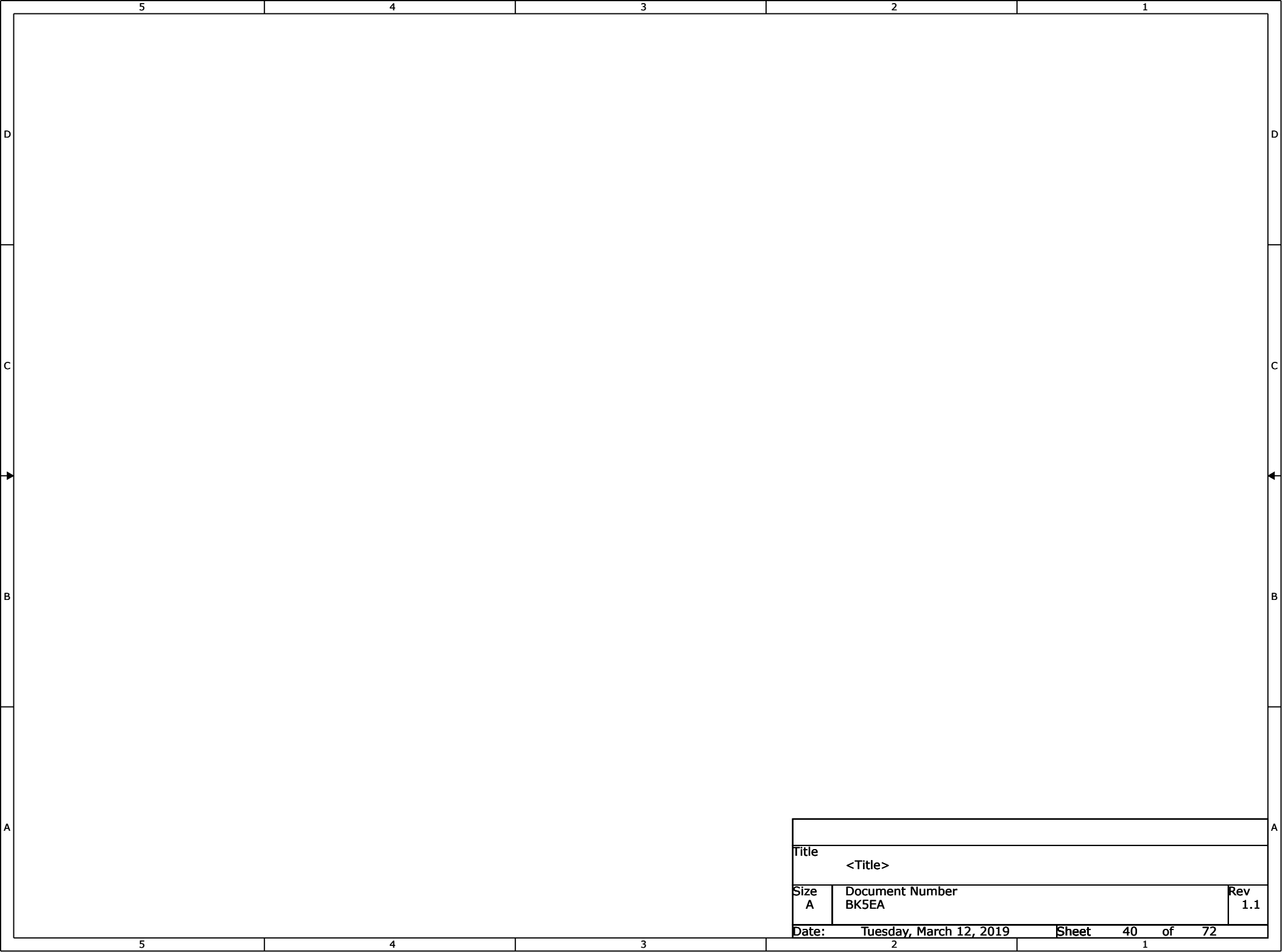
+AC_BAT_SYS  +AC_BAT_SYS 45,80,81,82,83,84,88,97



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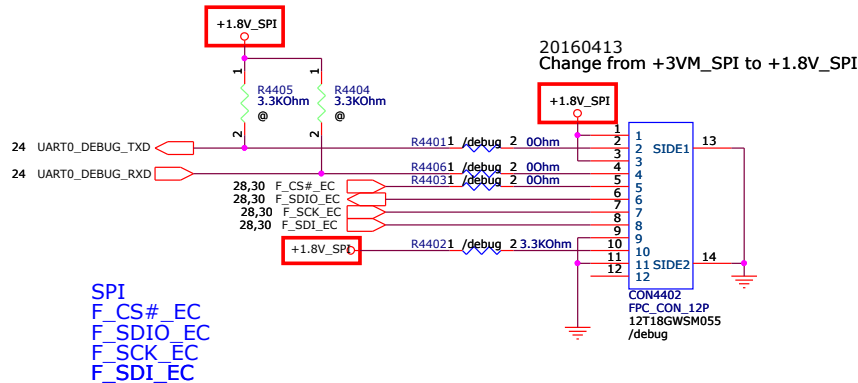
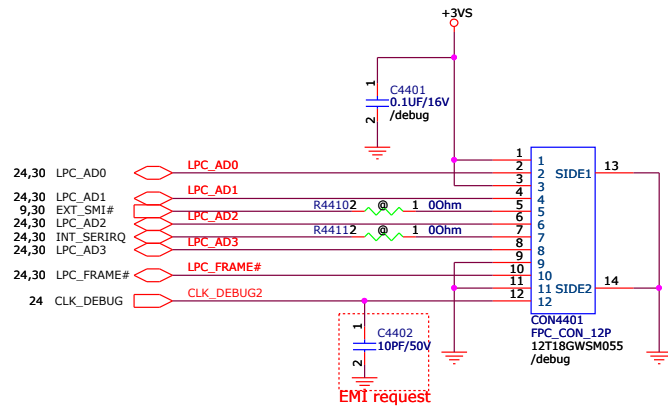
Title		
<Title>		
Size A	Document Number BK5EA	Rev 1.1
Date:	Tuesday, March 12, 2019	Sheet 38 of 72



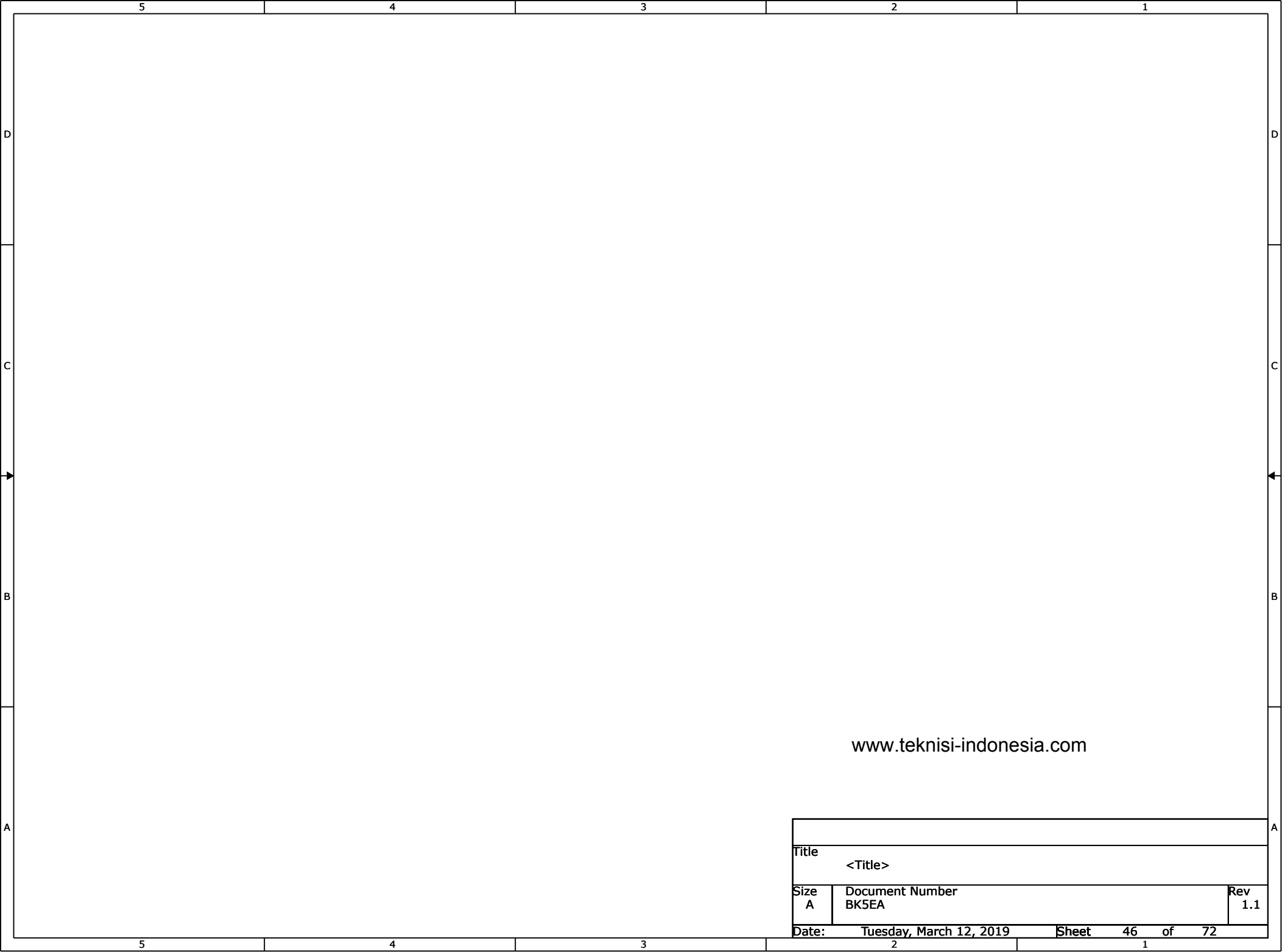


Title			
<Title>			
Size	Document Number		Rev
A	BK5EA		1.1
Date:	Tuesday, March 12, 2019	Sheet	40 of 72
	2		1

+3VS +3VS 8,9,11,16,24,30,31,32,33,36,38,45,48,50,51,57,74,87,89,91,92,96
+3VSUS +3VSUS 9,11,12,23,24,30,31,33,36,42,51,53,74,81,88,92,96
+3VM_SPD +3VM_SPI



SPI
F_CS#_EC
F_SDIO_EC
F_SCK_EC
F_SDI_EC

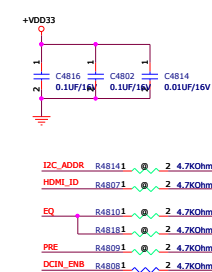
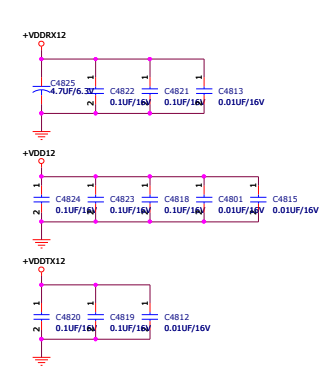
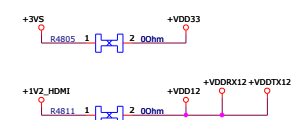
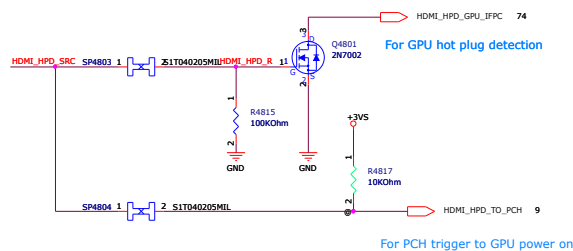
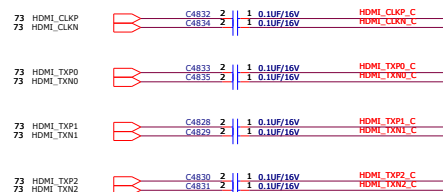


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<Title>			
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[illegible]

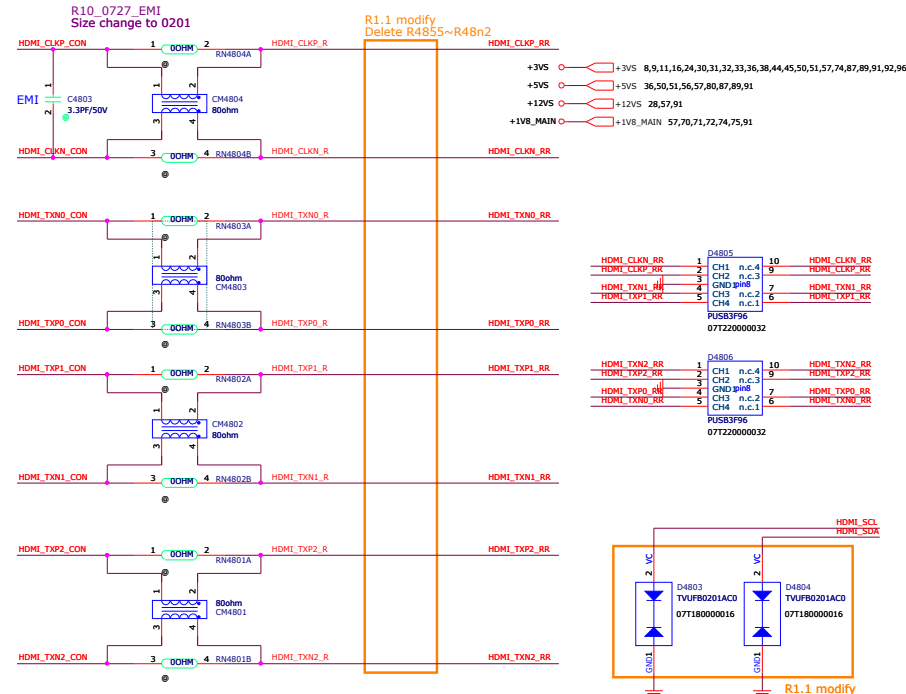
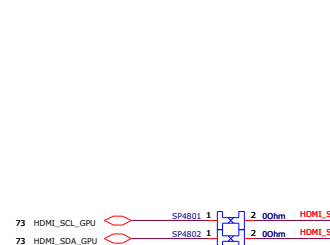
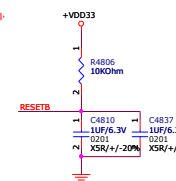
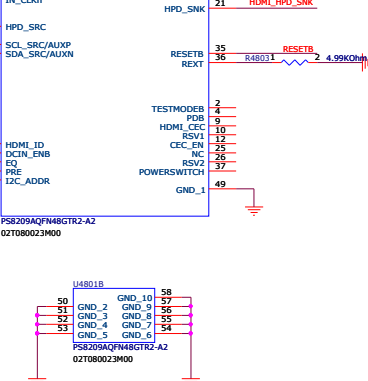
HDMI



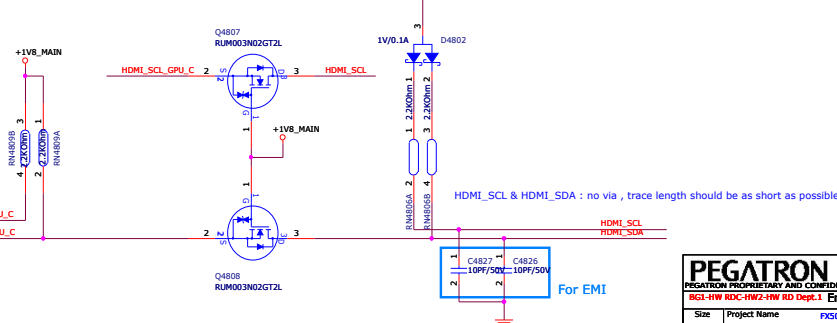
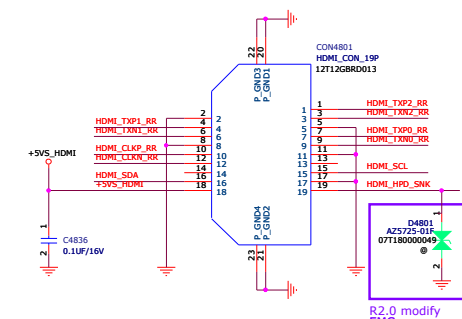
I2C slave address selection; Internal pull down
L: Default, Slave address 0x10-2F
H: Alternative slave address 0x90-9F; 0xD0-DF

HDMI ID enable; Internal pull down
L: Default, HDMI ID enable
H: HDMI ID disable

EQ -- Receiver equalization setting; Internal pull up
L: Compensation for channel loss up to 13db
H: Default, compensation for channel loss up to 17db
M: Compensation for channel loss up to 11db
PRE -- Output preemphasis setting; Internal pull up
L: Pre-emphasis = 2.5db
H: Default. No Pre-emphasis



20180102-1
Change CM Size to 0504
00hm to 0402



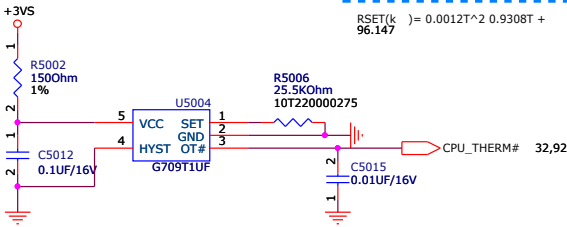


<Variant Name>			
PEGATRON		Title : eMMC	
BG1-HW3 RD		Engineer: Jack_Lee	
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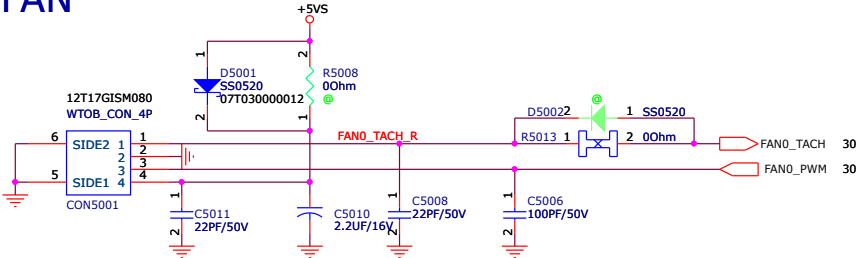
CPU Thermal Sensor

temperature set=85 C

$$RSET(k) = 0.0012T^2 + 0.9308T + 96.147$$

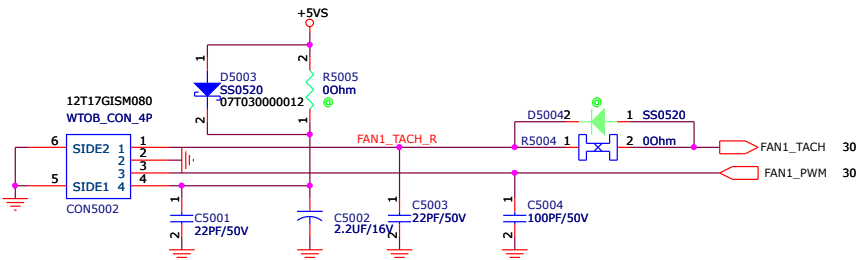


CPU FAN



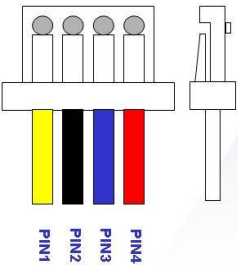
EC(PU@+3VS,10Kohm

GPU FAN



EC(PU@+3VS,10Kohm

4Pins Fan Connector Pins Definition



Pin No.	Function
Pin 1	TACHO
Pin 2	GNA
Pin 3	PWM
Pin 4	+5V

SSD/HDD

M.2 2280 KEY-M

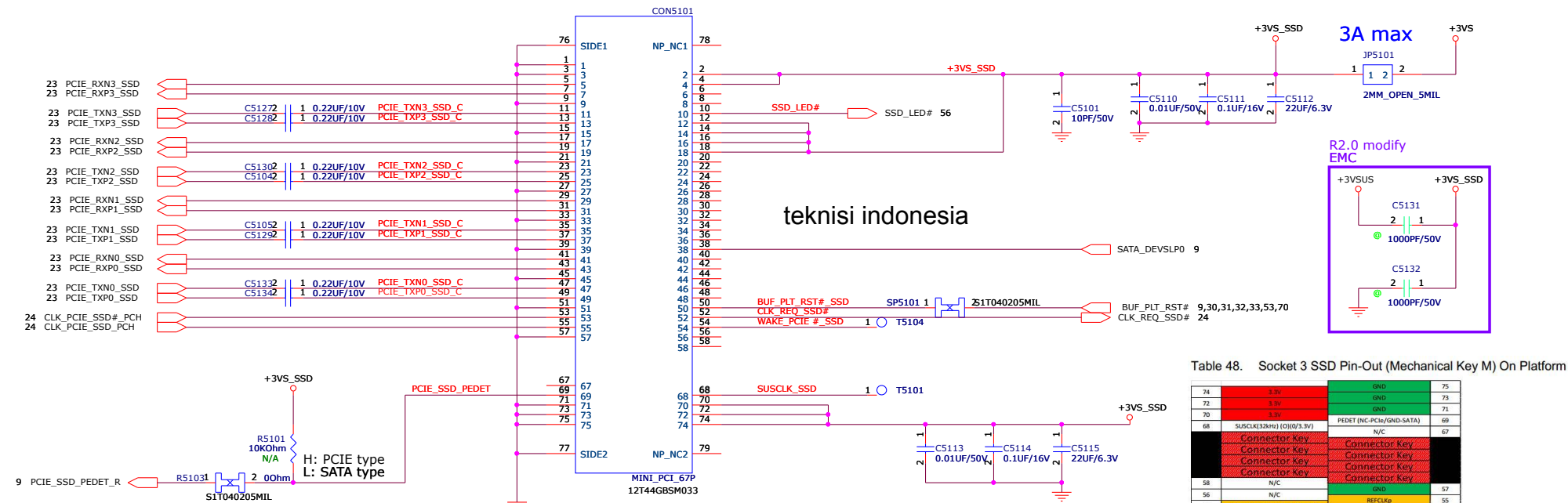
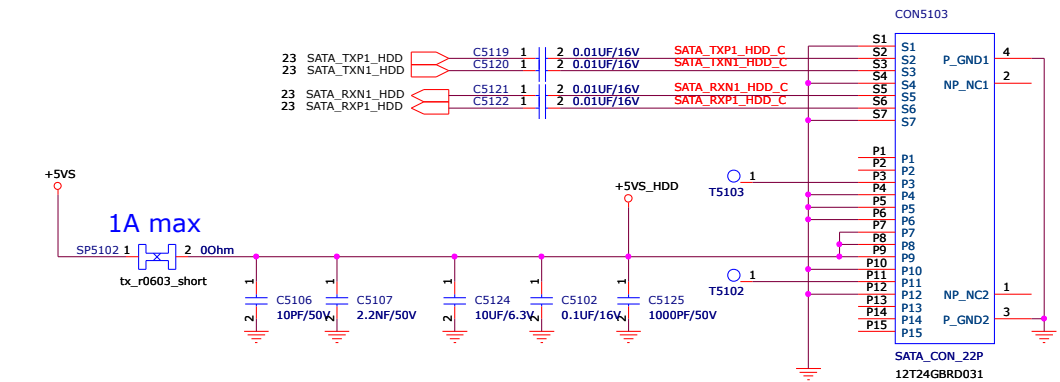


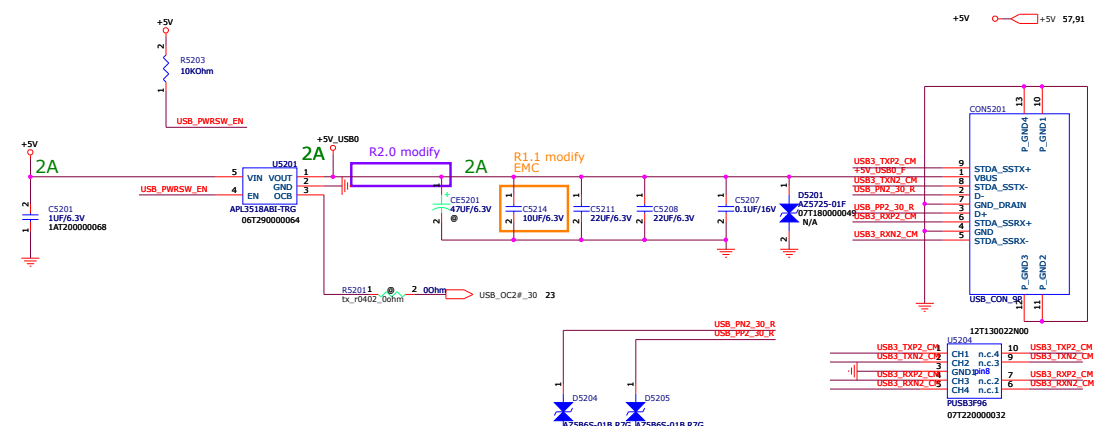
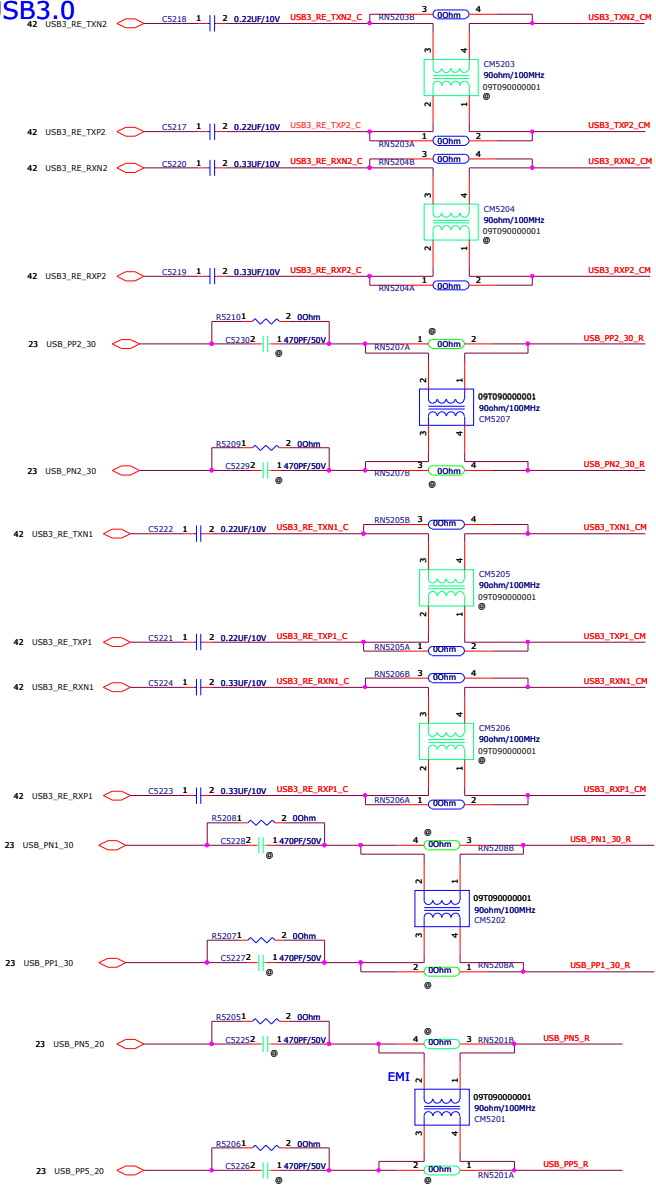
Table 48. Socket 3 SSD Pin-Out (Mechanical Key M) On Platform

74	3.3V	GROUND	75
72	3.3V	GROUND	73
70	3.3V	GROUND	71
68	SUSCLK(32MHz) (IO)/0(3.3V)	PEDET (NC-PCIE/GND-SATA)	69
		N/C	67
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
	Connector Key	Connector Key	
58	N/C	GROUND	57
56	N/C	REFCLKp	55
54	PERMANER (I/O)/0(3.3V) or N/C	REFCLKn	53
52	CLKREQ0 (I/O)/0(3.3V) or N/C	GROUND	51
50	PERSTR (IO)/0(3.3V) or N/C	PETpQ/SATA-A+	49
48	N/C	PETHQ/SATA-A+	47
46	N/C	GROUND	45
44	N/C	PETHQ/SATA-B+	43
42	N/C	PERnQ/SATA-B+	41
40	N/C	GROUND	39
38	DEVSLP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GROUND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GROUND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GROUND	21
20	N/C	PETp3	19
18	3.3V	PERn2	17
16	3.3V	GROUND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DA5/0SSA (I/O)/LED1# (I/O)/3.3V	GROUND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GROUND	3
2	3.3V	GROUND	1

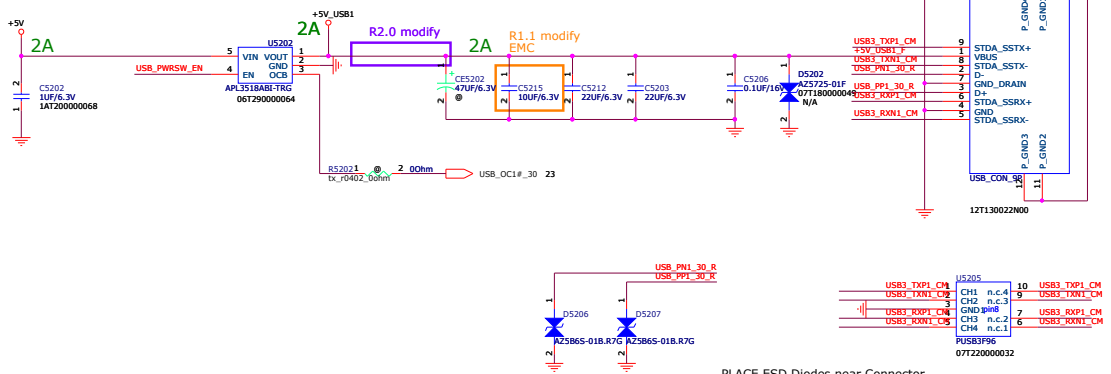
SATA Conn. 2.5"HDD



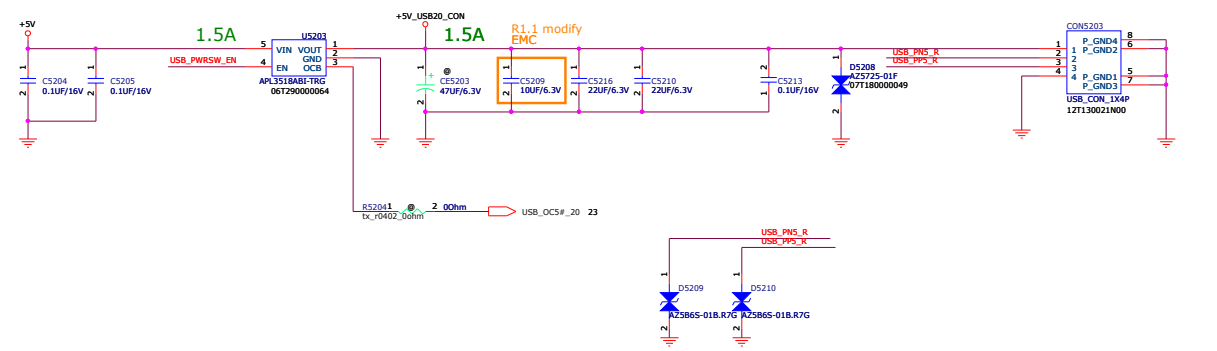
52.USB3.0



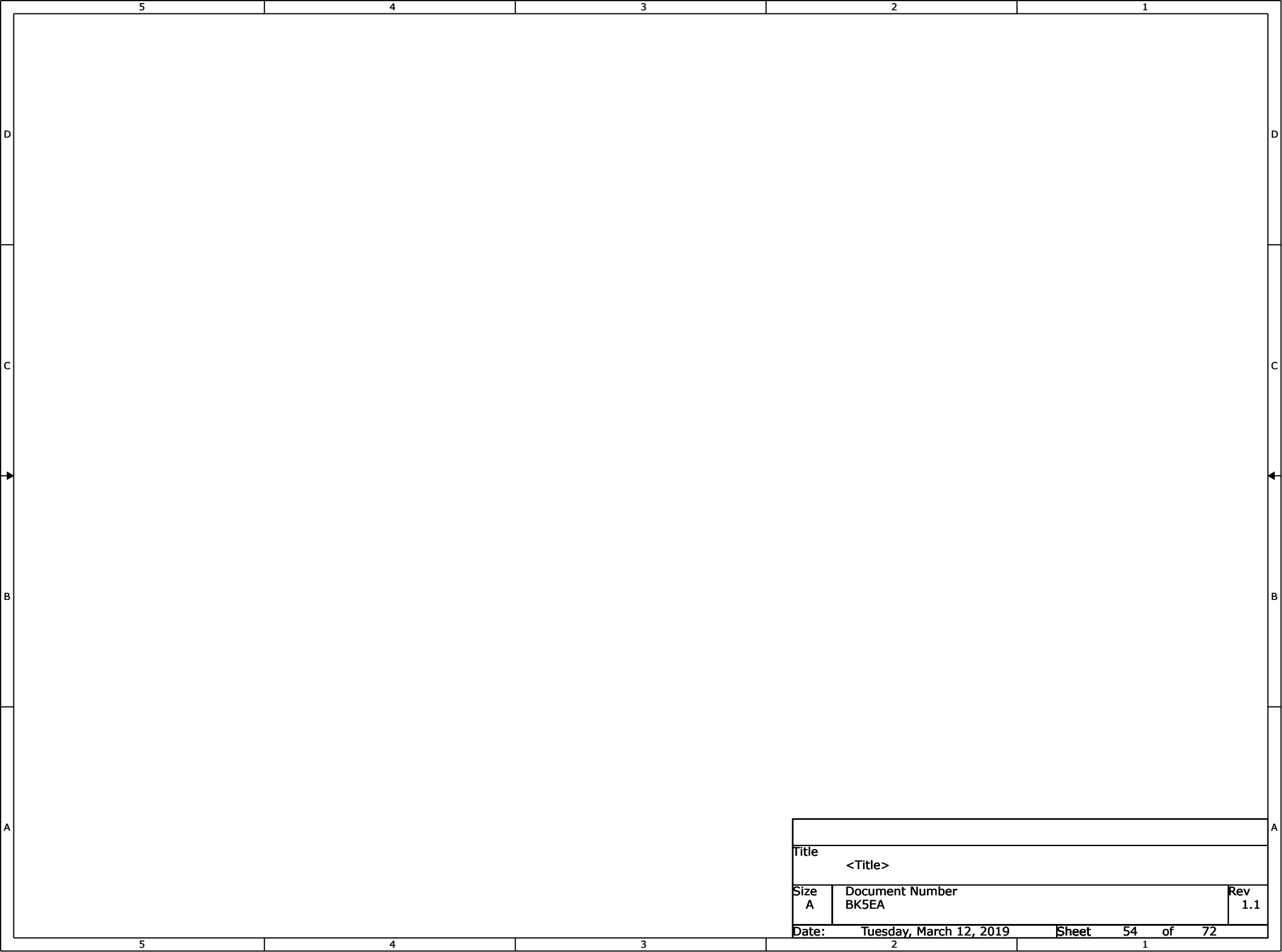
PLACE ESD Diodes near Connector



PLACE ESD Diodes near Connector



PLACE ESD Diodes near Connector



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<Title>				
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<Title>		
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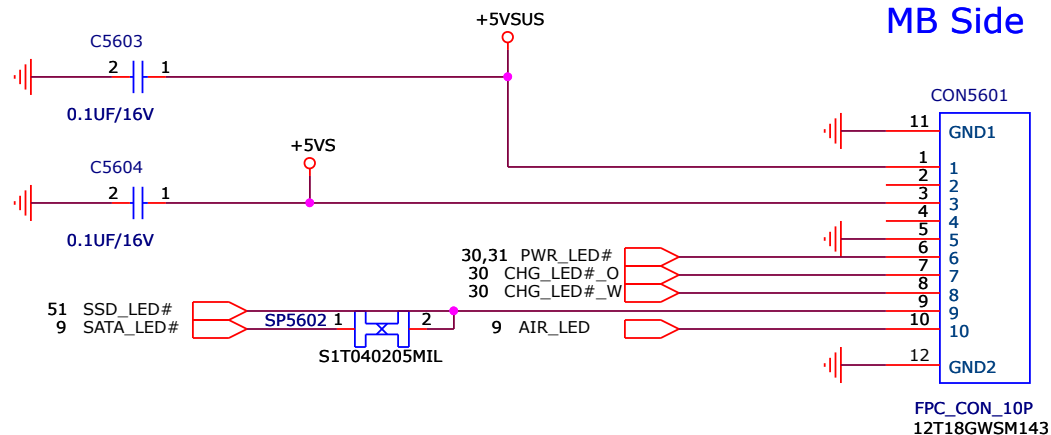
5

4

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2

1



+5VSUS 11,31,81
 +5VS 36,48,50,51,57,80,87,89,91

Power LED

AIR PLANE LED

NOTE: AIR_LED#_R
 High -> airplane mode ON -> LED ON
 Low -> airplane mode OFF -> LED OFF

Charger LED

PCB/ID LOCATION

PWR LED
LED5601

Charger LED
LED5606

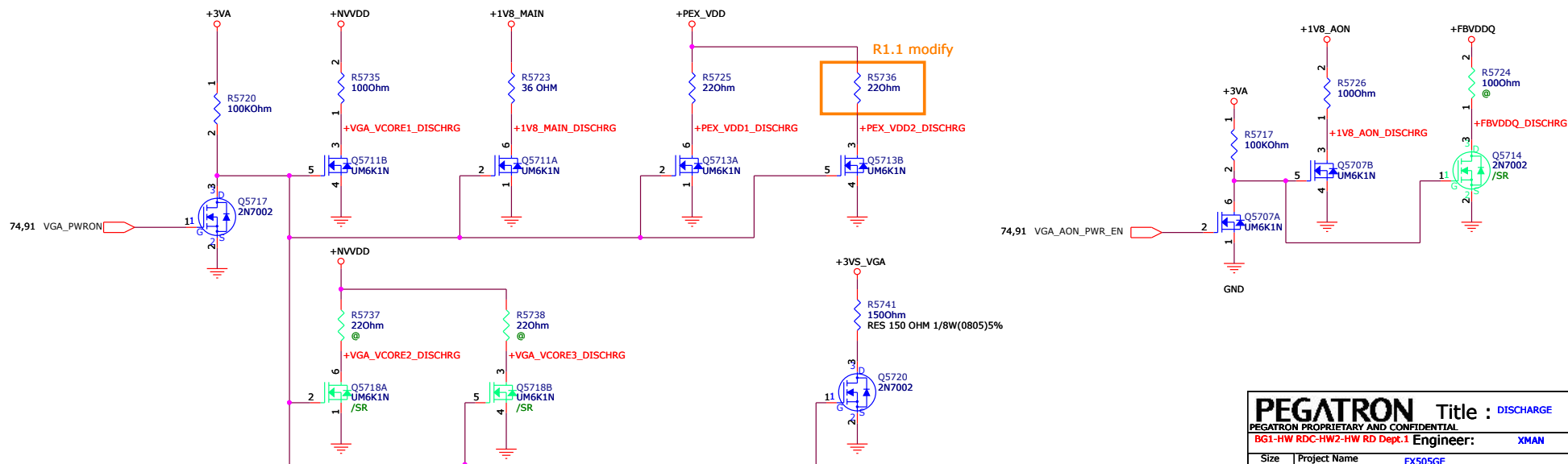
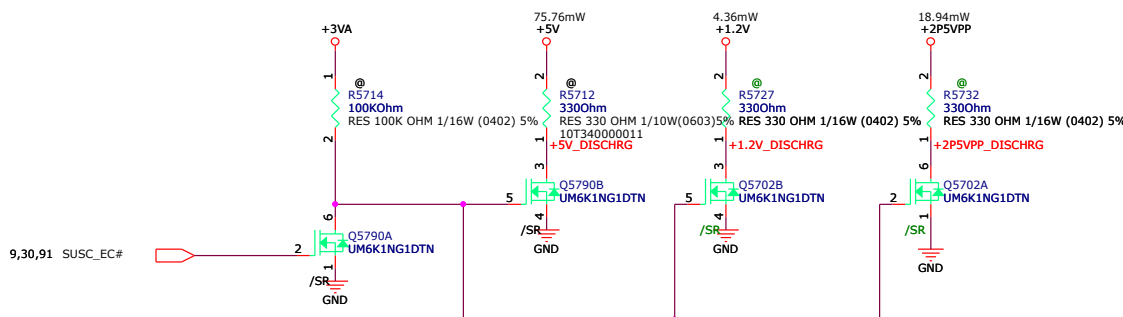
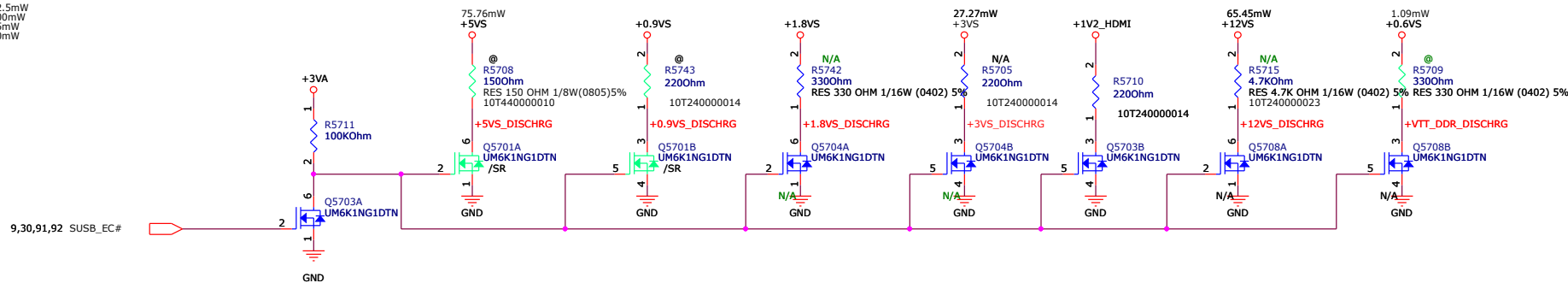
HDD LED
LED5604

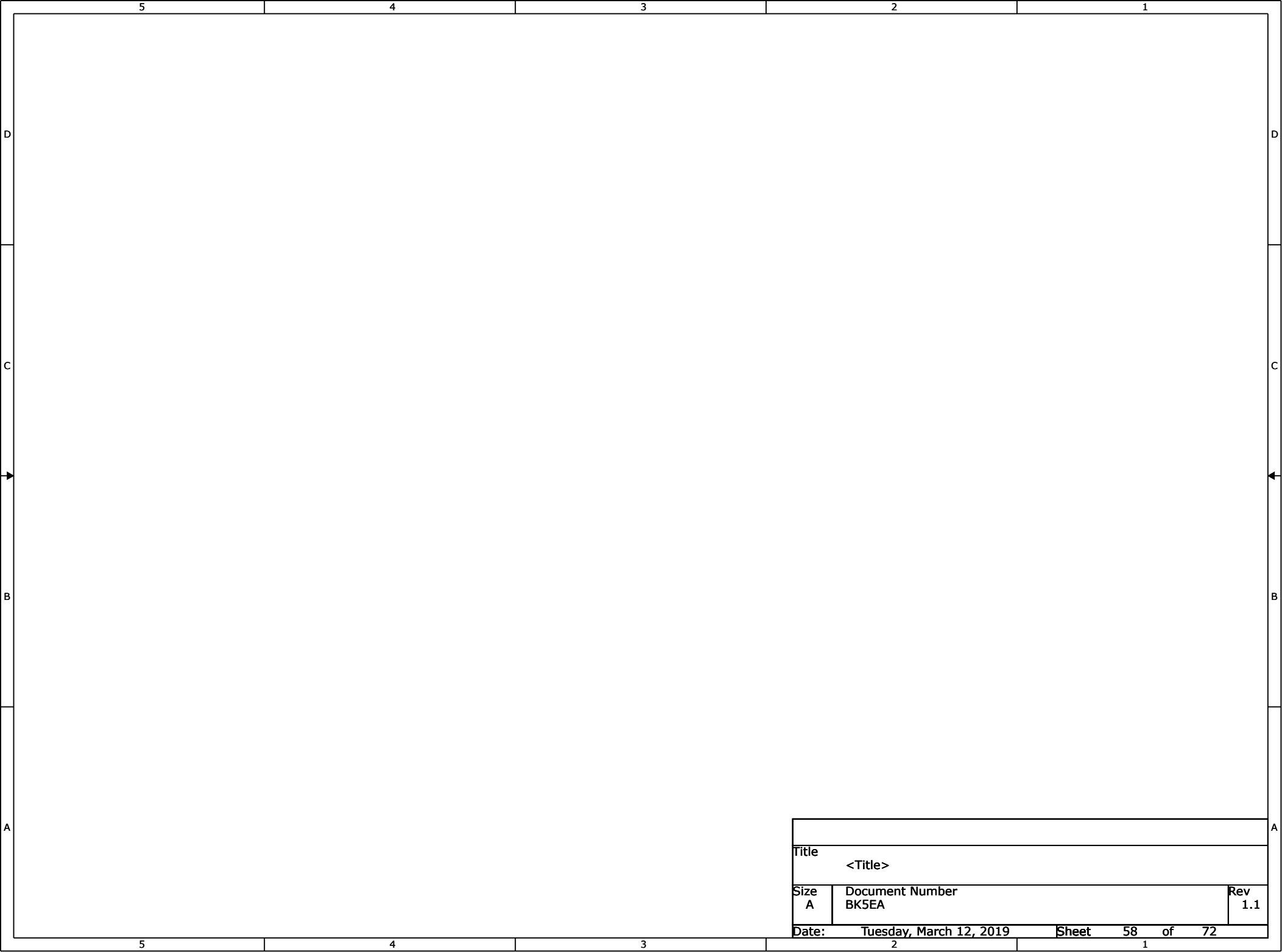
RF LED
LED5602

HDD LED

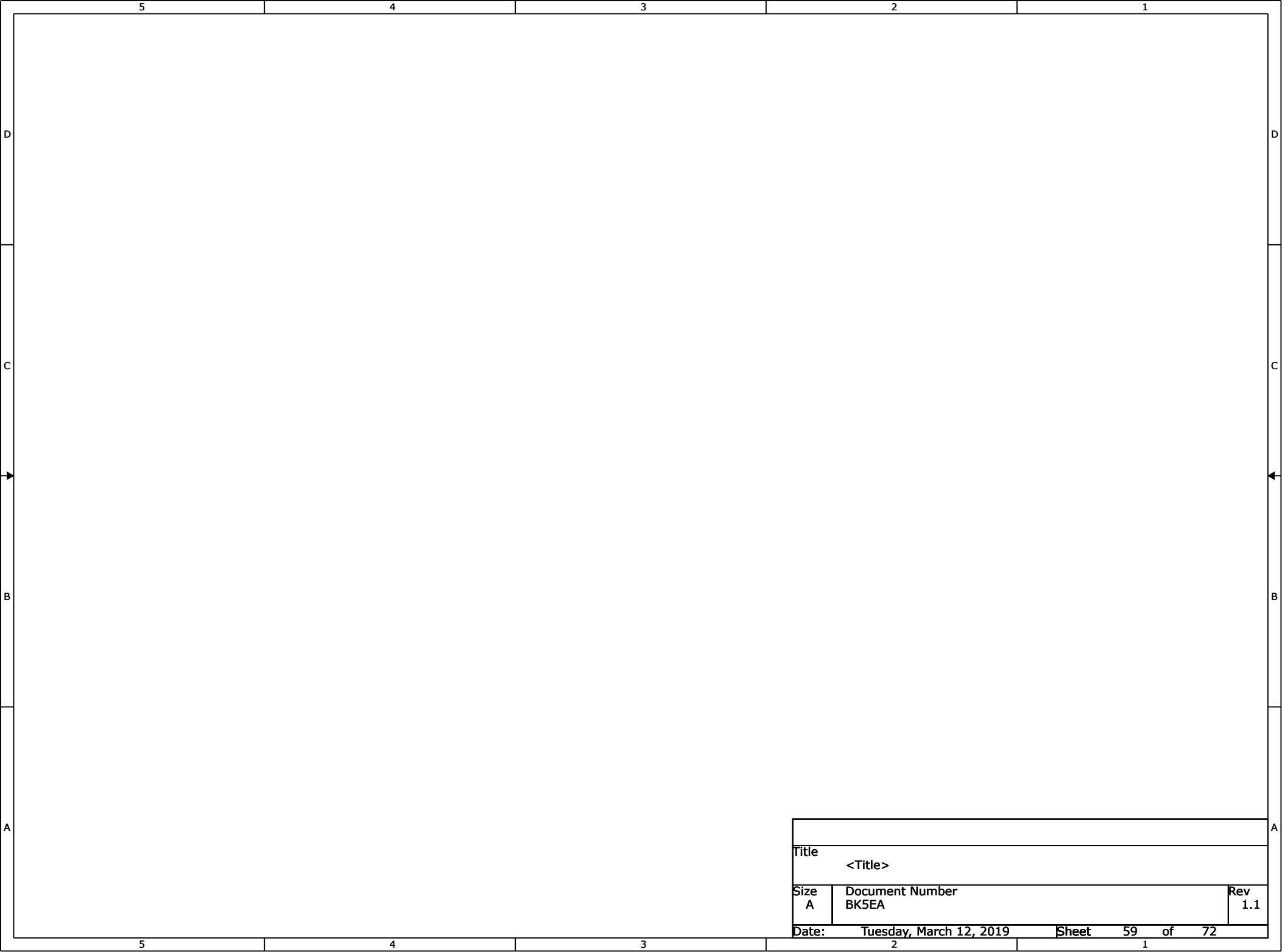
PEGATRON		Title : LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1-HW RDC-HW2-HW RD Dept.		Engineer: XMAN	
Size A4	Project Name Tuesday, March 12, 2019	Rev 56 72	1.0
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V^2/R
 0402 = 1/16W = 62.5mW
 0603 = 1/10W = 100mW
 0805 = 1/8W = 125mW
 1206 = 1/4W = 250mW



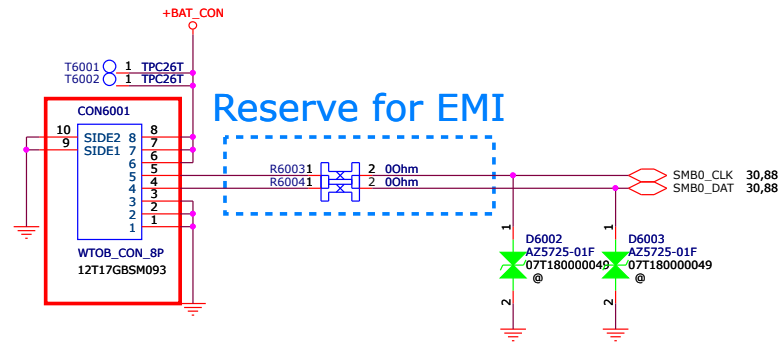


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<Title>				
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	2		1	



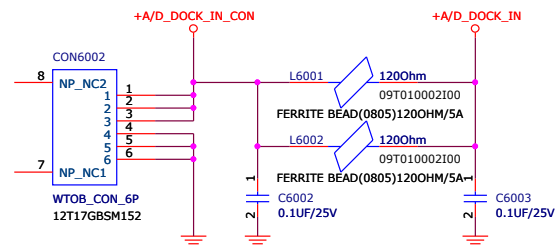
Title			
<Title>			
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	2		1

Battery Conn.

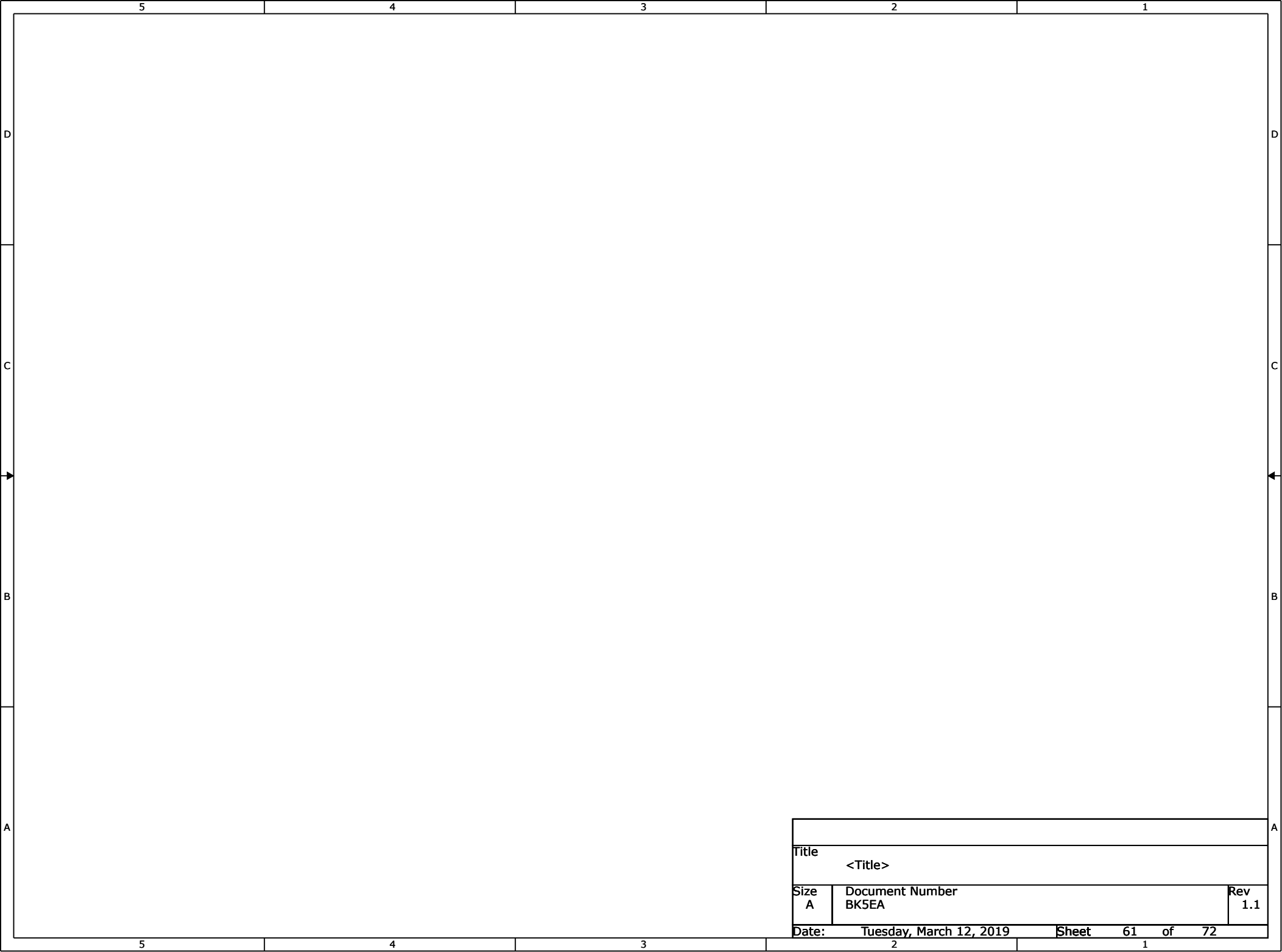


ABBA assign: 1217-01UG0AS(1217-017L000) doesn't include 1217-01EG000 (the same pool)

AC in Conn.



FX505GE N17P Adaptor: 120W
FX505GM N17E Adaptor: 150W



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A

A

<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Title USB 2.0 Hub

CONFIDENTIAL

Engineer: Jack_Lee

Size
A

Project Name	BK5EA
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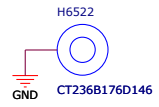
Rev
1.1

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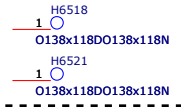
n5.NUT,Screw hole,Tooling hole

M.2 SSD NUT:



Tooling hole

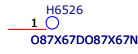
drill 3*3.5



drill 1.7

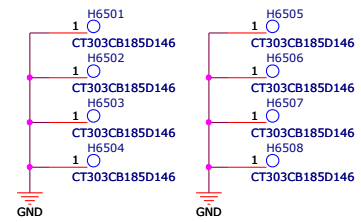


drill 2.2*1.7

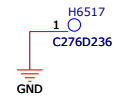


Screw hole

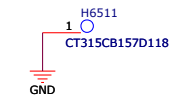
B group:
CPU GPU bracket hole



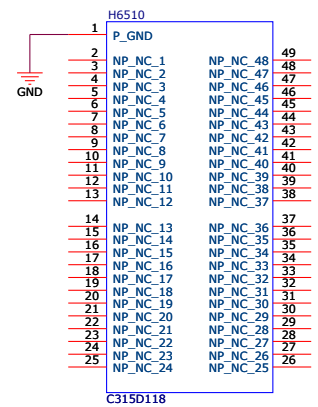
E:
TOP: phi 7 drill 6
BOT: phi 7 drill 6



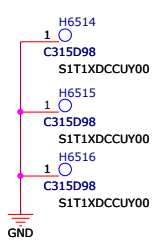
F:
TOP: phi 8 drill 3
BOT: phi 4 drill 3



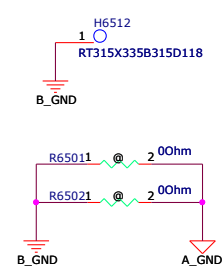
D group:



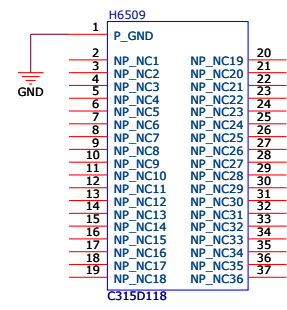
C group:
TOP: phi 8 drill 2.5
BOT: phi 8 drill 2.5



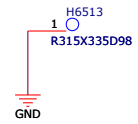
Near Audio Jack
TOP: square 8
BOT: phi 8 drill 3



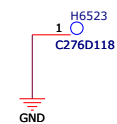
H group:



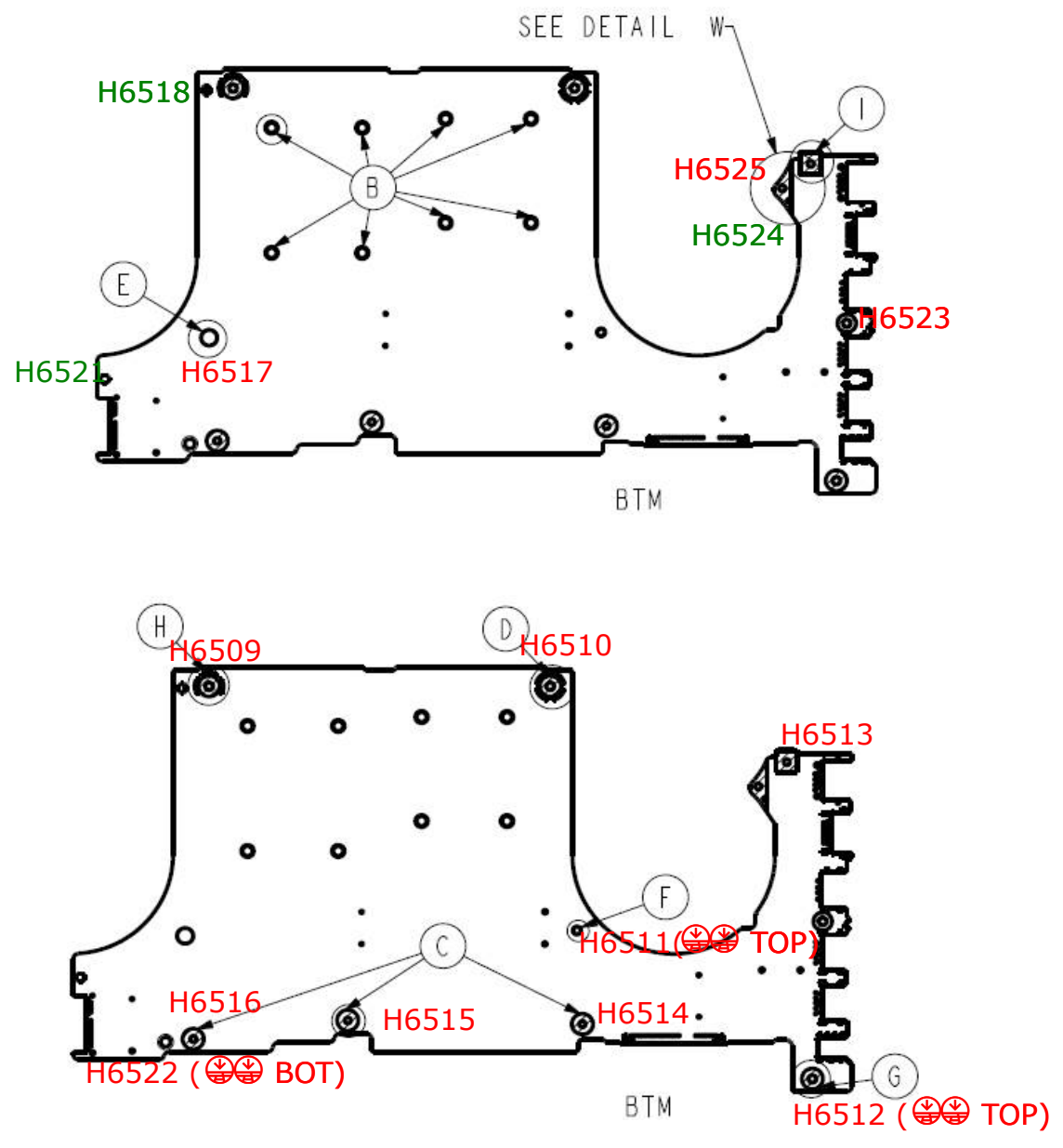
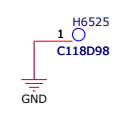
I group:
TOP: square8*8.5 drill 2.5
BOT: square8*8.5 drill 2.5



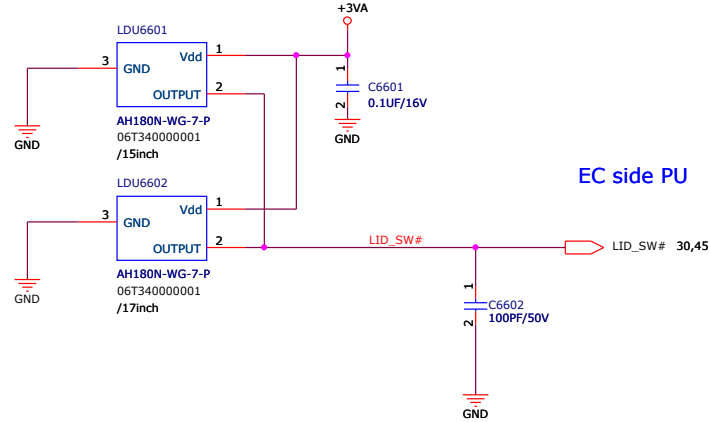
TOP: phi 7 drill 3
BOT: phi 7 drill 3



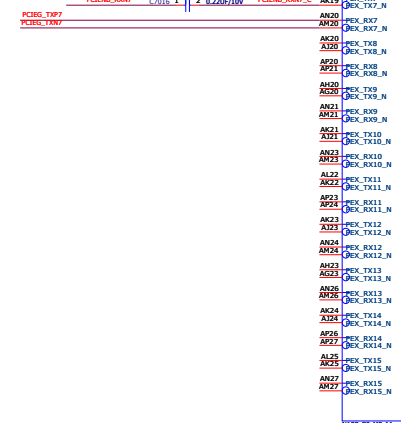
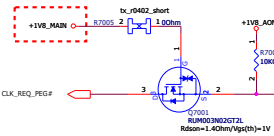
TOP: phi 3 drill 2.5
BOT: phi 3 drill 2.5



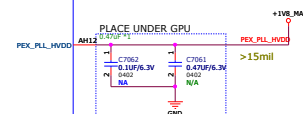
Hall sensor



EC side PU



23 PCIENB_RXP[0..7]



GPU	Capacitor Type	Footprint	Population	N18	N17	Location
PEV_HYDIO Supply Rail						
GB4C-128, GB4D-128	1.0 μ F	X85	0402 or 0203	0	4	Under GPU
	0.47 μ F	X85	0204V16	32	0	Under GPU
	4.7 μ F	X85	0204V16	2	0	Heat Sink
	4.7 μ F	X85	0603	3	0	Under GPU
	10 μ F	X58	0805	0	1	Midway between GPU and power supply
	10 μ F	X85	0805	3	0	Heat Sink
	22 μ F	X58	0805	0	1	Midway between GPU and power supply
	22 μ F	X85	0805	2	0	Heat Sink
PEV_HYDIO Supply Rail						
GB4C-128, GB4D-128	1.0 μ F	X85	0402 or 0203	0	4	Under GPU
	0.47 μ F	X85	0204V16	14	0	Under GPU
	4.7 μ F	X85	0603	0	2	Heat Sink
	4.7 μ F	X85	0805	3	0	Under GPU
	10 μ F	X3B	0805	0	2	Midway between GPU and power supply
	10 μ F	X85	0805	3	0	Heat Sink
	22 μ F	X58	0805	0	1	Midway between GPU and power supply
	22 μ F	X85	0805	2	0	Heat Sink

Note:

1. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F.

GPU	Capacitor Type	Footprint	Population		Location	
			N18	N17		
PEX_PLL_HVDD Supply Rail						
GB4C-128, GB4D-128	0.1 μ F	X7R	0402	0	1	Under GF
	0.47 μ F ¹	X6S	0201W	1	0	Under GF

Note:

- Decoupling for PEX_PLL_HVDD is merged with PEX_HVDD, and Design may alternatively use type 0201W 0.47 μ F X6S for each 0201W 1 μ F.

Rail (GPU Ball)	Balls	Voltage	Filtering under GPU	Filtering Near GPU
PEX_HVDD	14	1.8V	14 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) ----- <u>Alternate solution:</u> 7 x 1uF (0402 or 0201W, X6S) ³ 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)
PEX_DVDD	6	1.0V	12 x 0.47uF (0201W X6S) 3 x 4.7uF (0603 X6S) ----- <u>Alternate solution:</u> 6 x 1uF (0402 or 0201W, X6S) ³ 3 x 4.7uF (0603 X6S)	3 x 10uF (0805 X6S) 2 x 22uF (0805 X6S)

+PEX_VDD 57,76,73,96
+1VB_MAIN 48,57,76,71,74,75,91

NVIDIA (N17P)
DA-07679-001_v05 P.37

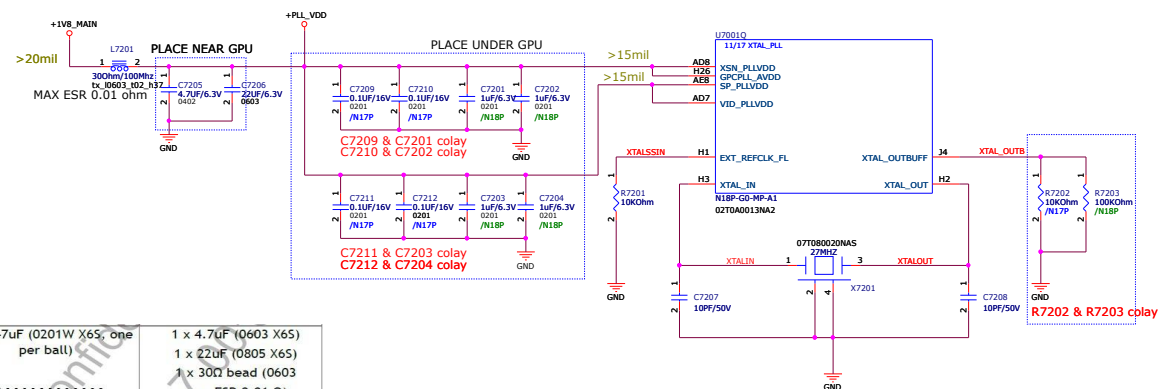
XS_PLLVDD
Under GPU (Put at GPCPLL_AVDD side)
No capacitors

NVIDIA (N17P)
DA-07679-001_v05 P.38

SP_PLLVDD/VID_PLLVDD
Under GPU
0.1uF x2 (0402)

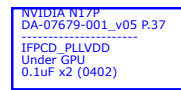
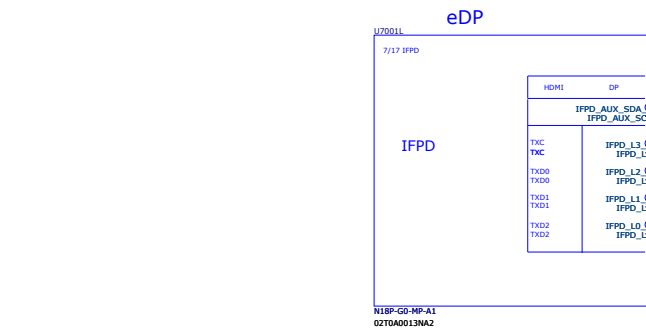
NVIDIA (N17P)
DA-07679-001_v05 P.38

GPCPLL_AVDD
Under GPU
0.1uF x1 (0402)
Near GPU
4.7uF x1 (0603)
22 uF x1 (0805)



IFPAB_PLLVDD	1	1.8V	3 x 0.47uF (0201W X6S, one per ball)	1 x 4.7uF (0603 X6S)
IFPCD_PLLVDD	1			1 x 22uF (0805 X6S)
IFPE_PLLVDD	1			1 x 30Ω bead (0603 max ESR 0.01 Ω)
GPCPLL_AVDDx	2		2 x 0.47uF (0201W X6S)	
XS_N_PLLVDD			Alternate solution: 3 x 1uF (0402 or 0201W, X6S, one per ball)	
SP_PLLVDD	1		2 x 1uF (0402 or 0201W, X6S)	
VID_PLLVDD	1		1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	
			Alternate solution: 1 x 0.47uF (0201W X6S)	
			Alternate solution: 1 x 1uF (0402 or 0201W, X6S)	

Capacitor	Value	ESR	Location
IFPAB_PLLVDD	0.1 uF	0.005	Under GPU
IFPCD_PLLVDD	0.1 uF	0.005	Under GPU
IFPE_PLLVDD	0.1 uF	0.005	Under GPU
GPCPLL_AVDDx	0.1 uF	0.005	Under GPU
XS_N_PLLVDD	0.1 uF	0.005	Under GPU
SP_PLLVDD	0.1 uF	0.005	Under GPU
VID_PLLVDD	0.1 uF	0.005	Under GPU
XTALIN	0.1 uF	0.005	Under GPU
XTALOUT	0.1 uF	0.005	Under GPU
XTALOUTBUFF	0.1 uF	0.005	Under GPU
XTALOUTB	0.1 uF	0.005	Under GPU
XTALIN	0.1 uF	0.005	Under GPU
XTALOUT	0.1 uF	0.005	Under GPU
XTALOUTBUFF	0.1 uF	0.005	Under GPU
XTALOUTB	0.1 uF	0.005	Under GPU



GPU	Type	Footprint	Population	
			N18	N17
FP7_IDVD	Supply Rails			
GBAC-128	0.1 μF	X7R 0402	0	8
GB4D-128	0.47 μF	X6S 0201W	6	0
	1.0 μF	X6S 0402 or 0201W	6	3
	0.47 μF	X6S 0201W	6	0
	4.7 μF	X6S 0403	3	3
	Bead Type			
	180 Ω @ 100 MHz (ESR=0.2 Ω)	0403	0	0
				Hear GPU

Note:

1. Design may alternatively use one 0201W 0.47 μ F X65 for each 0201W 1 μ F
2. Design may alternatively use two 0201W 0.47 μ F X65 for each 0201W 1 μ F

If an IFP link is unused, in general it should be left unconnected. This includes Main and Aux links. IFPxy_RSET and IFPxy_PLLVDD (xy=AB,CD,EF) can be left unconnected if neither of IFPx /IFPy is in use.

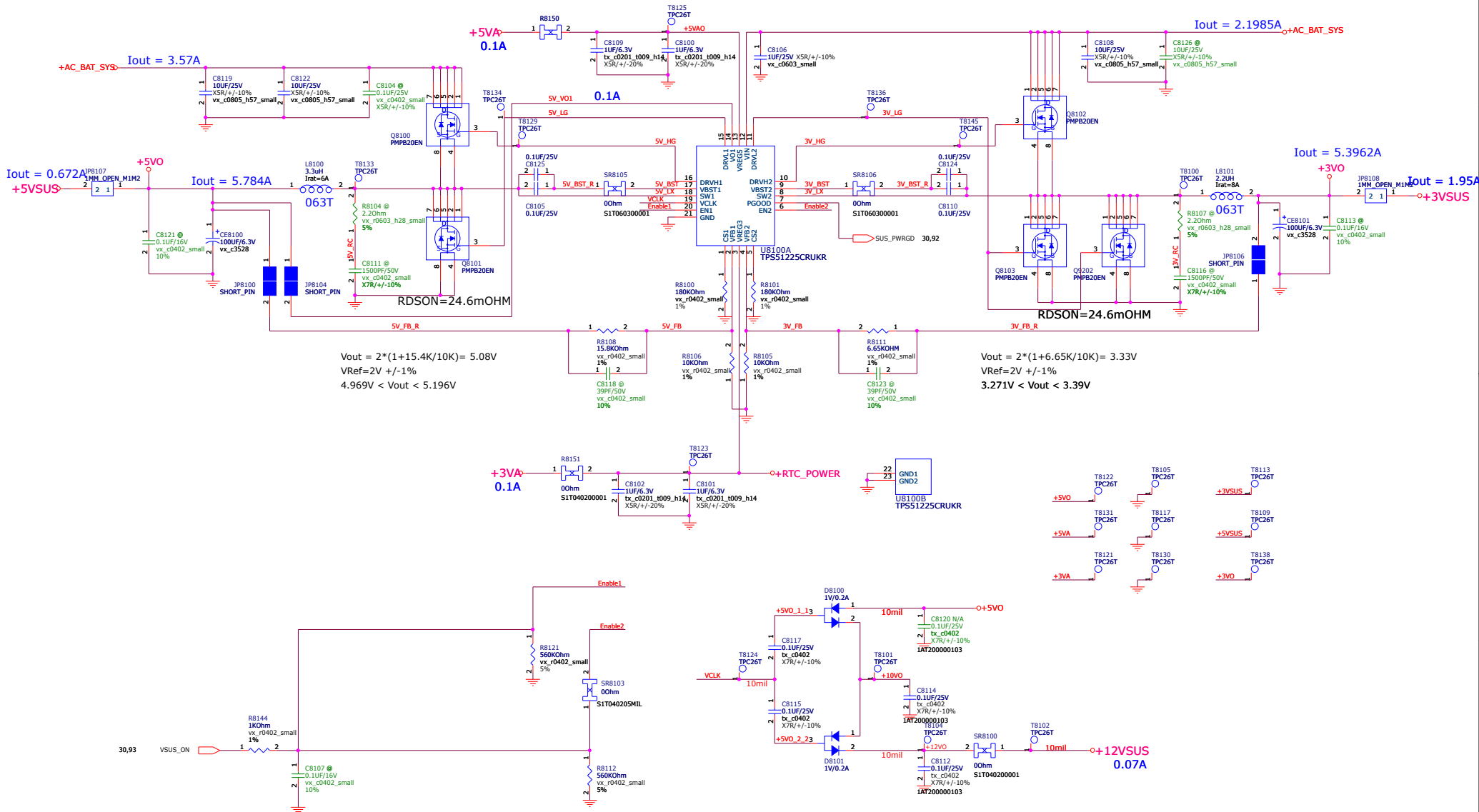
NVIDIA (N17P)
DA-07679-001_v05 P.36

IFP_IOVDD
Under GPU
0.1uF x6 (0402)
Near GPU
4.7uF x3 (0603)
1uF x3 (0402)

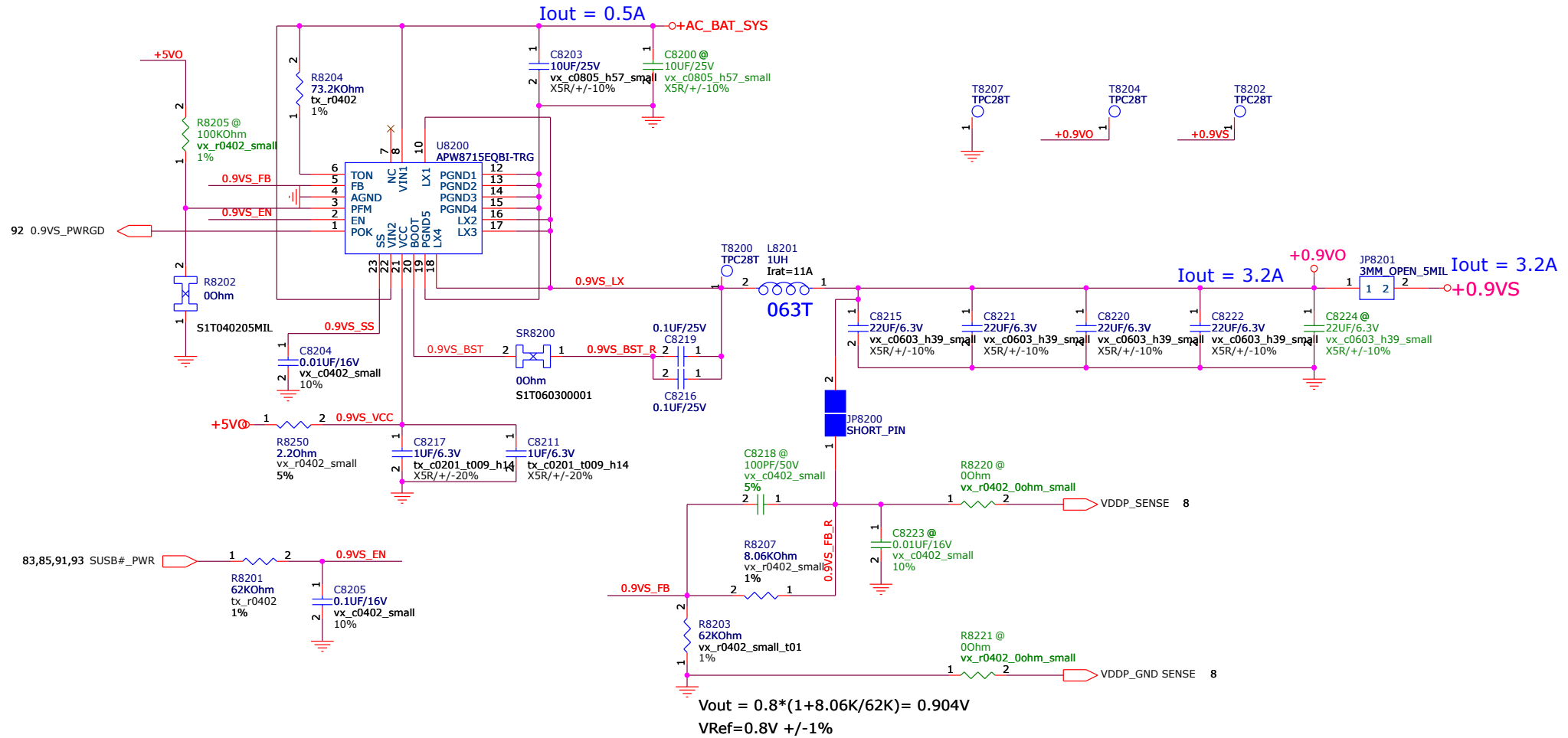
IFP_IOVDD	6	1.0V	$6 \times 0.47\mu\text{F}$ (0201W X65) <hr/> <u>Alternate solution:</u> $6 \times 1\mu\text{F}$ (0402 or 0201W, X65)	$6 \times 0.47\mu\text{F}$ (0201W X65) $3 \times 4.7\mu\text{F}$ (0603 X65) <hr/> <u>Alternate solution:</u> $3 \times 1\mu\text{F}$ (0402 or 0201W, X65) $3 \times 4.7\mu\text{F}$ (0603, X65) ³
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5VO & 3VO POWER SUPPLY

$V_{out} = 2 \cdot (1 + 6.65K/10K) = 3.33V$
 $V_{Ref} = 2V \pm 1\%$
 $3.271V < V_{out} < 3.39V$



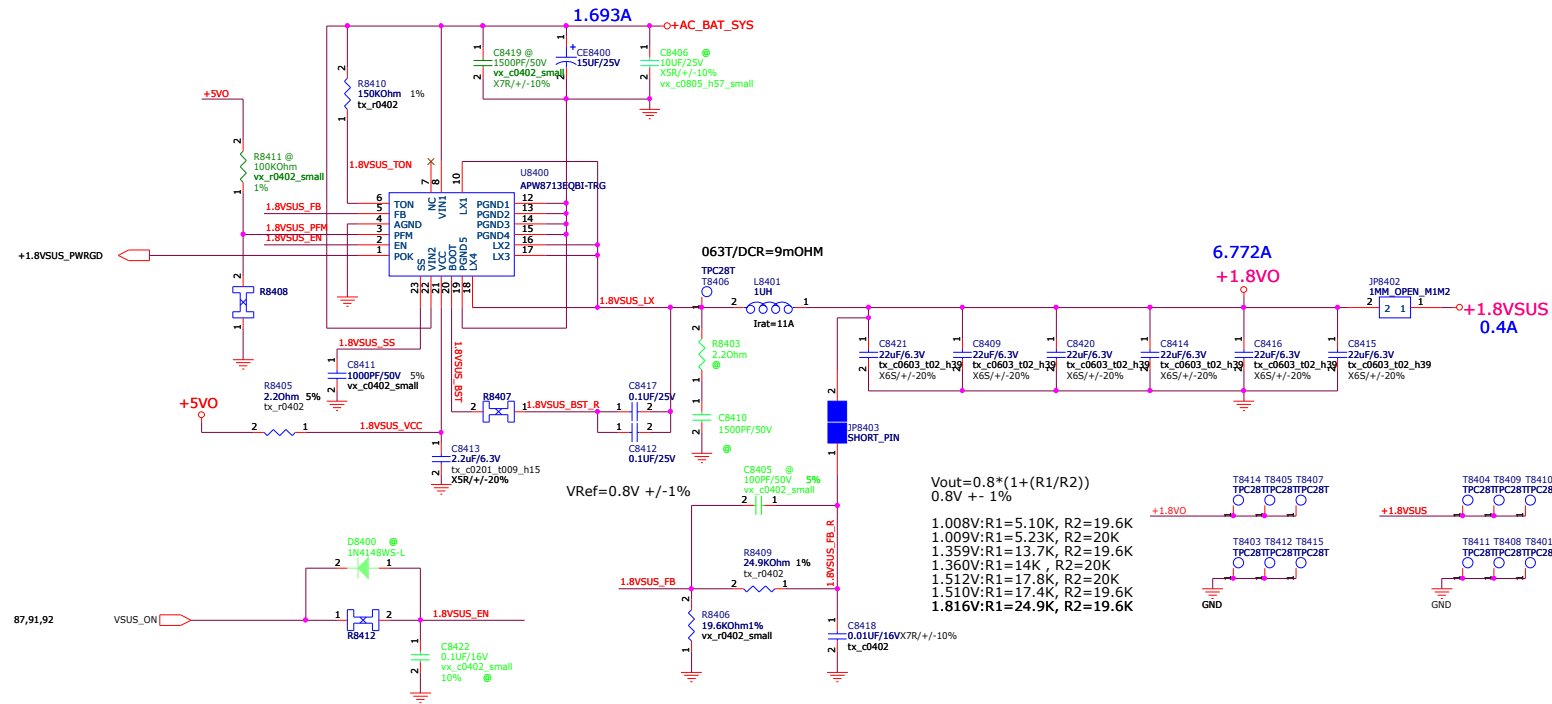
0.9VS POWER SUPPLY



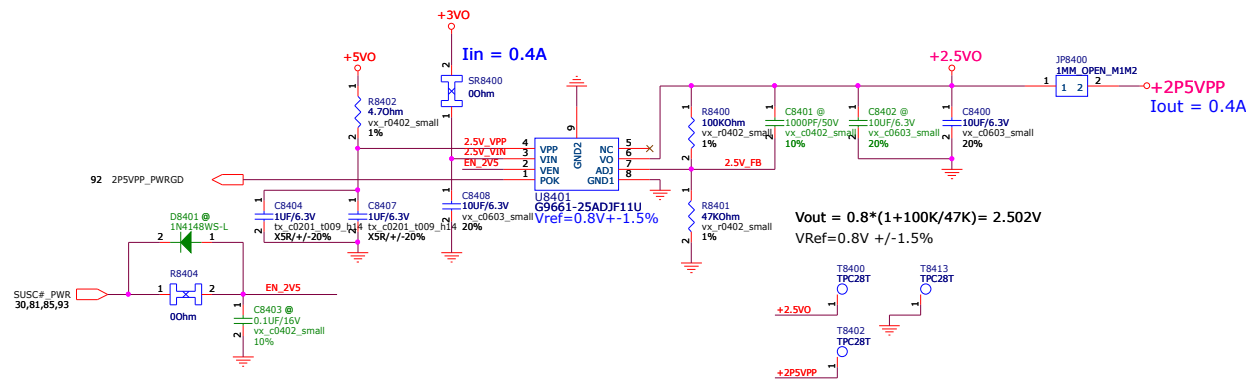
<Variant Name>

PEGATRON		Title : +0.9VS	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Wayne_Sung	
Size Custom	Project Name	FX505AN	
Date: Tuesday, March 12, 2019		Sheet	82 of 97
		Rev	1.0

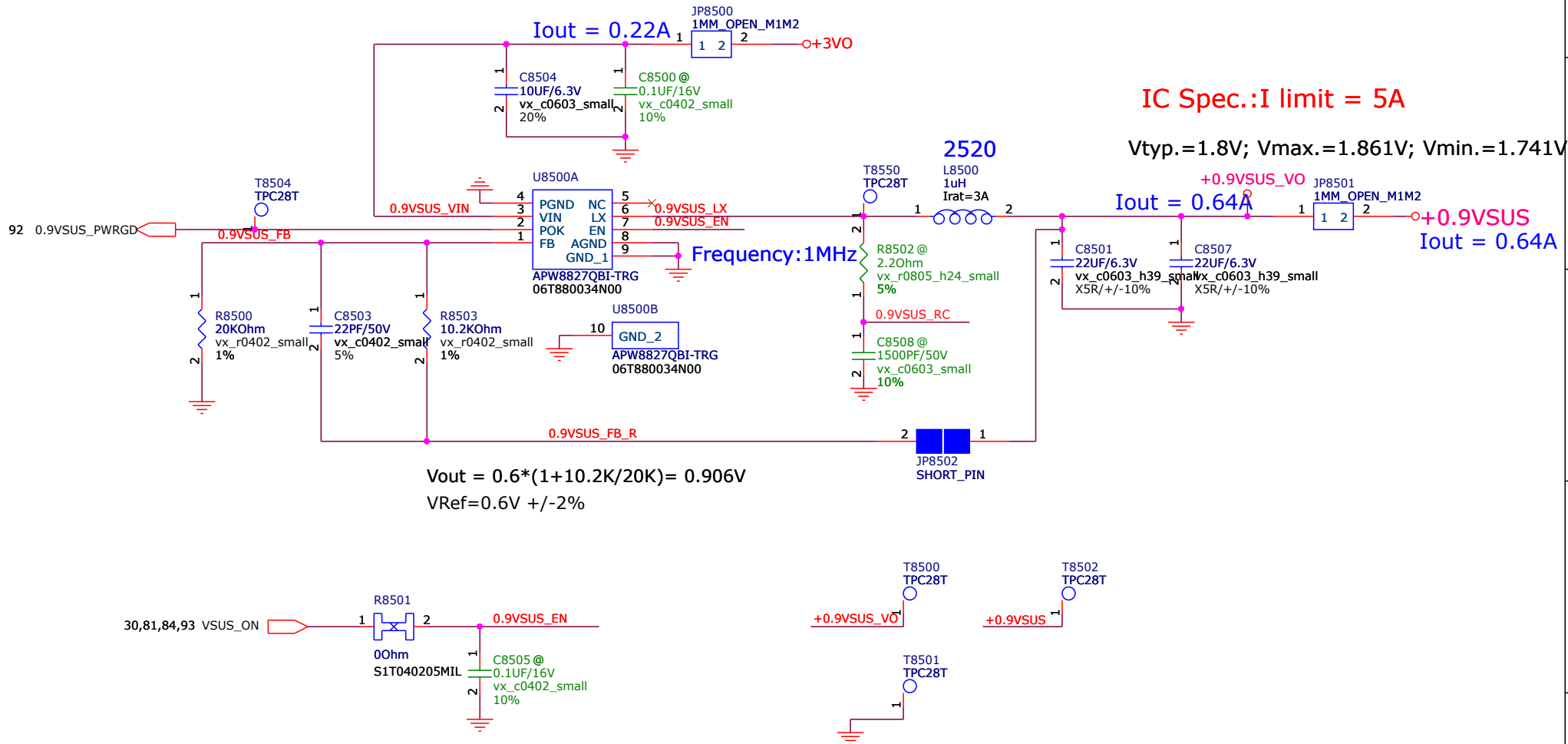
1.8VSUS POWER SUPPLY



2.5VO POWER SUPPLY

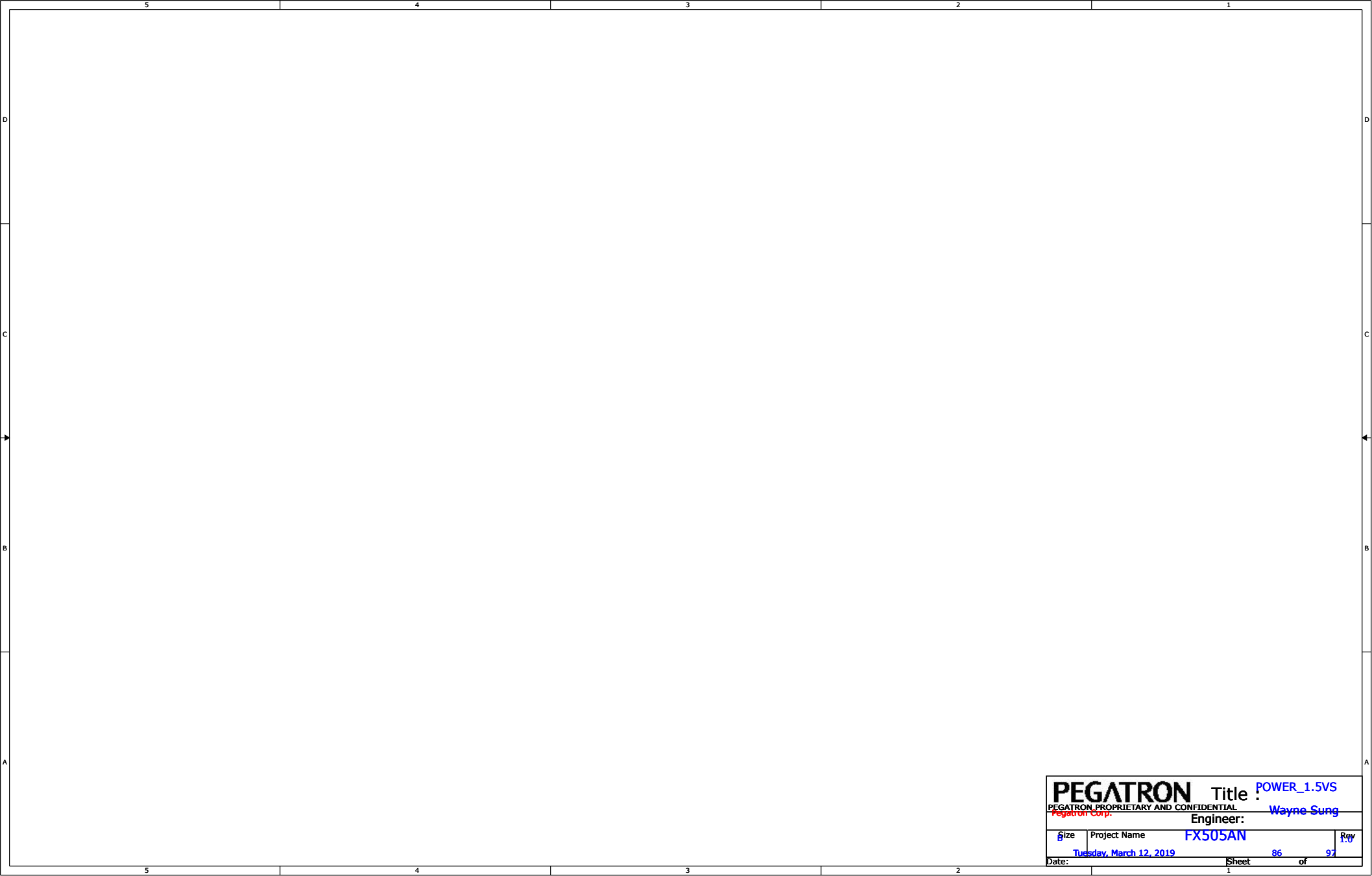


0.9VSUS POWER SUPPLY

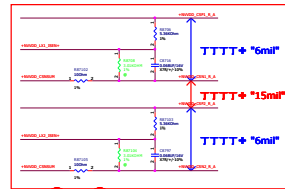
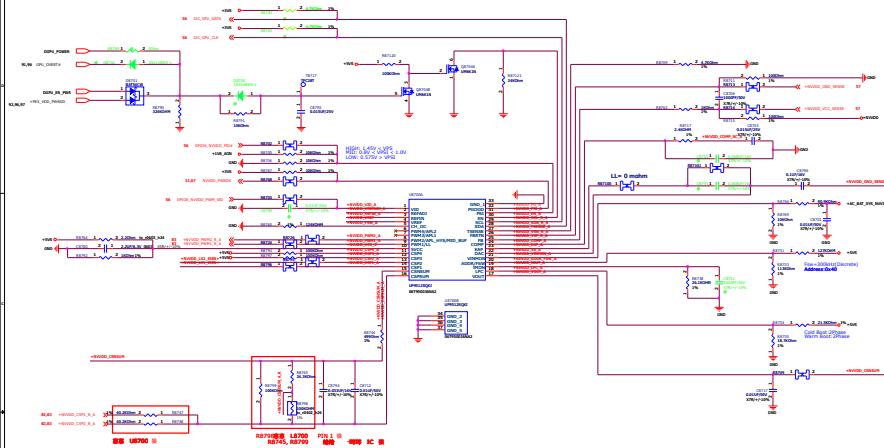


<Variant Name>

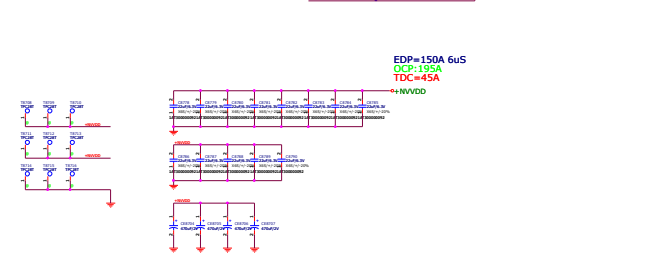
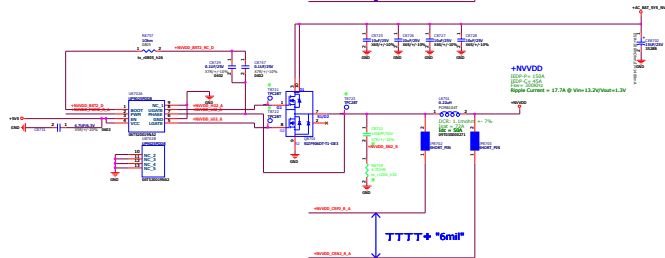
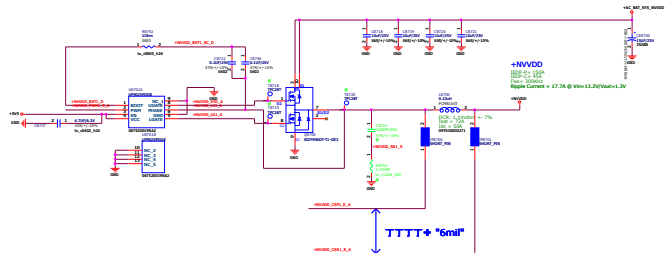
PEGATRON		Title : POWER_0.9VSUS	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: Wayne Sung	
Size Custom	Project Name FX505AN		Rev 1.0
Date: Tuesday, March 12, 2019	Sheet 85 of 97		



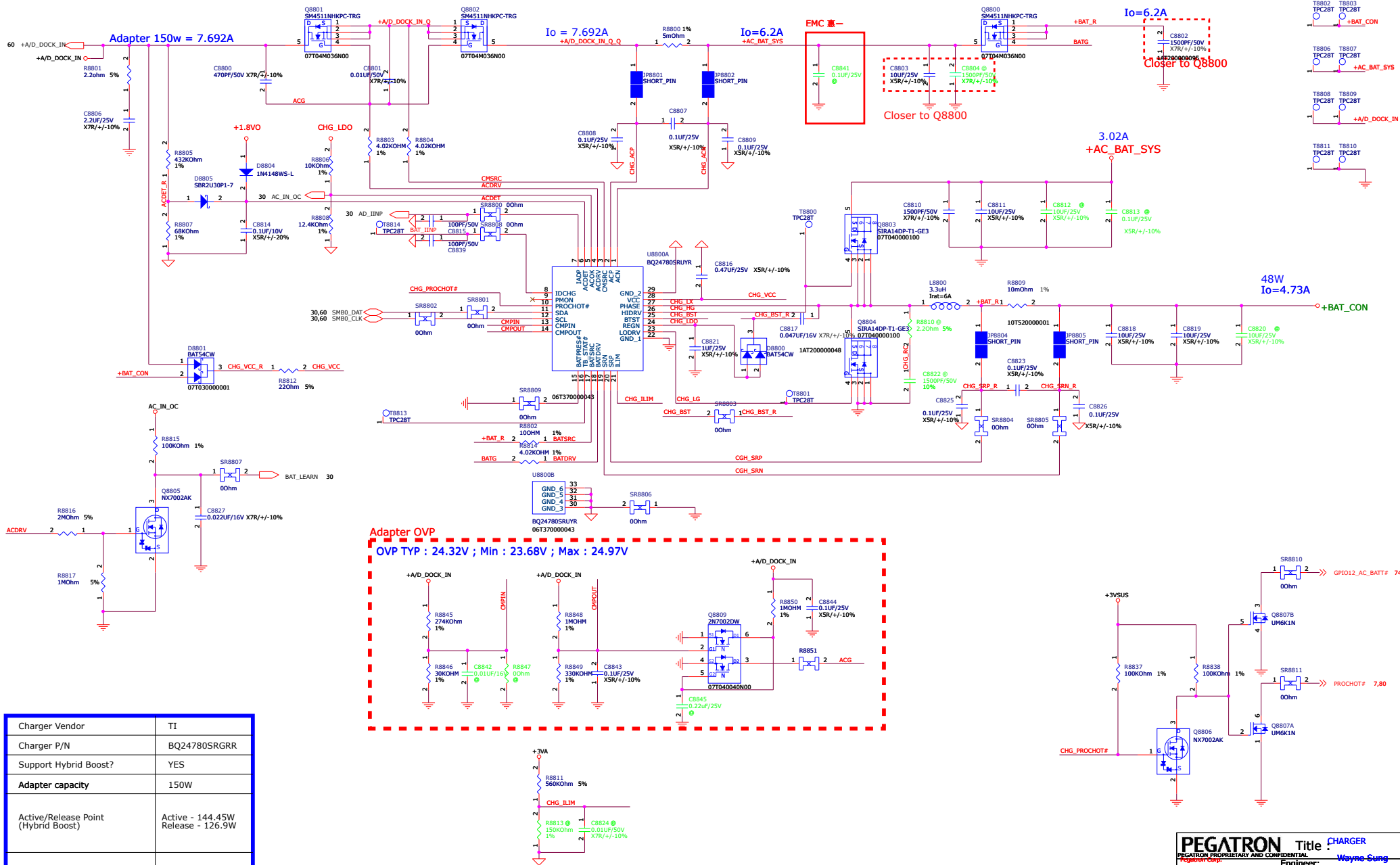
PEGATRON		Title :		POWER_1.5VS
PEGATRON PROPRIETARY AND CONFIDENTIAL				
Pegatron Corp.		Engineer:		Wayne Sung
Size	Project Name	FX505AN	Rev	1.1
Date: Tuesday, March 12, 2019		Sheet	86	of 97



叫U8700



BATTERY CHARGER



Charger Vendor	TI
Charger P/N	BQ24780SRGRR
Support Hybrid Boost?	YES
Adapter capacity	150W
Active/Release Point (Hybrid Boost)	Active - 144.45W Release - 126.9W
Enable condition Disable condition	RSOC>40% RSOC<30%